DAQ

DAQPad™-6070E
User Manual

Multifunction I/O Device for 1394 Bus Computers

April 2002 Edition
Part Number 322205B-01

Worldwide Technical Support and Product Information

ni.com

National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 683 0100

Worldwide Offices

Australia 03 9879 5166, Austria 0662 45 79 90 0, Belgium 02 757 00 20, Brazil 011 3262 3599,
Canada (Calgary) 403 274 9391, Canada (Montreal) 514 288 5722, Canada (Ottawa) 613 233 5949,
Canada (Québec) 514 694 8521, Canada (Toronto) 905 785 0085, China (Shanghai) 021 6555 7838,
China (ShenZhen) 0755 3904939, Czech Republic 02 2423 5774, Denmark 45 76 26 00, Finland 09 725 725 11,
France 01 48 14 24 24, Germany 089 741 31 30, Greece 30 1 42 96 427, Hong Kong 2645 3186,
India 91 80 4190000, Israel 03 6393737, Italy 02 413091, Japan 03 5472 2970, Korea 02 3451 3400,
Malaysia 603 9596711, Mexico 001 800 010 0793, Netherlands 0348 433466, New Zealand 09 914 0488,
Norway 32 27 73 00, Poland 0 22 3390 150, Portugal 351 210 311 210, Russia 095 238 7139,
Singapore 6 2265886, Slovenia 386 3 425 4200, South Africa 11 805 8197, Spain 91 640 0085,
Sweden 08 587 895 00, Switzerland 056 200 51 51, Taiwan 02 2528 7227, United Kingdom 01635 523545

For further support information, see the *Technical Support and Professional Services* appendix. To comment on the documentation, send email to techpubs@ni.com.

© 1999–2002 National Instruments Corporation. All rights reserved.

Important Information

Warranty

The DAQPad-6070E is warranted against defects in materials and workmanship for a period of one year from the date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

The media on which you receive National Instruments software are warranted not to fail to execute programming instructions, due to defects in materials and workmanship, for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace software media that do not execute programming instructions if National Instruments receives notice of such defects during the warranty period. National Instruments does not warrant that the operation of the software shall be uninterrupted or error free.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. National Instruments will pay the shipping costs of returning to the owner parts which are covered by warranty.

National Instruments believes that the information in this document is accurate. The document has been carefully reviewed for technical accuracy. In the event that technical or typographical errors exist, National Instruments reserves the right to make changes to subsequent editions of this document without prior notice to holders of this edition. The reader should consult National Instruments if errors are suspected. In no event shall National Instruments be liable for any damages arising out of or related to this document or the information contained in it.

EXCEPT AS SPECIFIED HEREIN, NATIONAL INSTRUMENTS MAKES NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. CUSTOMER'S RIGHT TO RECOVER DAMAGES CAUSED BY FAULT OR NEGLIGENCE ON THE PART OF NATIONAL INSTRUMENTS SHALL BE LIMITED TO THE AMOUNT THERETOFORE PAID BY THE CUSTOMER. NATIONAL INSTRUMENTS WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. This limitation of the liability of National Instruments will apply regardless of the form of action, whether in contract or tort, including negligence. Any action against National Instruments must be brought within one year after the cause of action accrues. National Instruments shall not be liable for any delay in performance due to causes beyond its reasonable control. The warranty provided herein does not cover damages, defects, malfunctions, or service failures caused by owner's failure to follow the National Instruments installation, operation, or maintenance instructions; owner's modification of the product; owner's abuse, misuse, or negligent acts; and power failure or surges, fire, flood, accident, actions of third parties, or other events outside reasonable control.

Copyright

Under the copyright laws, this publication may not be reproduced or transmitted in any form, electronic or mechanical, including photocopying, recording, storing in an information retrieval system, or translating, in whole or in part, without the prior written consent of National Instruments Corporation.

Trademarks

CVI™, DAQPad™, DAQ-STC™, IMAQ™, IVI™, LabVIEW™, Measurement Studio™, MITE™, MXI™, National Instruments™, NI™, ni.com™, NI-DAQ™, RTSI™, and SCXI™ are trademarks of National Instruments Corporation.

FireWire is a trademark of Apple Computer, Inc. Other product and company names mentioned herein are trademarks or trade names of their respective companies.

Patents

For patents covering National Instruments products, refer to the appropriate location: **Help»Patents** in your software, the `patents.txt` file on your CD, or `ni.com/patents`.

WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

(1) NATIONAL INSTRUMENTS PRODUCTS ARE NOT DESIGNED WITH COMPONENTS AND TESTING FOR A LEVEL OF RELIABILITY SUITABLE FOR USE IN OR IN CONNECTION WITH SURGICAL IMPLANTS OR AS CRITICAL COMPONENTS IN ANY LIFE SUPPORT SYSTEMS WHOSE FAILURE TO PERFORM CAN REASONABLY BE EXPECTED TO CAUSE SIGNIFICANT INJURY TO A HUMAN.

(2) IN ANY APPLICATION, INCLUDING THE ABOVE, RELIABILITY OF OPERATION OF THE SOFTWARE PRODUCTS CAN BE IMPAIRED BY ADVERSE FACTORS, INCLUDING BUT NOT LIMITED TO FLUCTUATIONS IN ELECTRICAL POWER SUPPLY, COMPUTER HARDWARE MALFUNCTIONS, COMPUTER OPERATING SYSTEM SOFTWARE FITNESS, FITNESS OF COMPILERS AND DEVELOPMENT SOFTWARE USED TO DEVELOP AN APPLICATION, INSTALLATION ERRORS, SOFTWARE AND HARDWARE COMPATIBILITY PROBLEMS, MALFUNCTIONS OR FAILURES OF ELECTRONIC MONITORING OR CONTROL DEVICES, TRANSIENT FAILURES OF ELECTRONIC SYSTEMS (HARDWARE AND/OR SOFTWARE), UNANTICIPATED USES OR MISUSES, OR ERRORS ON THE PART OF THE USER OR APPLICATIONS DESIGNER (ADVERSE FACTORS SUCH AS THESE ARE HEREAFTER COLLECTIVELY TERMED "SYSTEM FAILURES"). ANY APPLICATION WHERE A SYSTEM FAILURE WOULD CREATE A RISK OF HARM TO PROPERTY OR PERSONS (INCLUDING THE RISK OF BODILY INJURY AND DEATH) SHOULD NOT BE RELIANT SOLELY UPON ONE FORM OF ELECTRONIC SYSTEM DUE TO THE RISK OF SYSTEM FAILURE. TO AVOID DAMAGE, INJURY, OR DEATH, THE USER OR APPLICATION DESIGNER MUST TAKE REASONABLY PRUDENT STEPS TO PROTECT AGAINST SYSTEM FAILURES, INCLUDING BUT NOT LIMITED TO BACK-UP OR SHUT DOWN MECHANISMS. BECAUSE EACH END-USER SYSTEM IS CUSTOMIZED AND DIFFERS FROM NATIONAL INSTRUMENTS' TESTING PLATFORMS AND BECAUSE A USER OR APPLICATION DESIGNER MAY USE NATIONAL INSTRUMENTS PRODUCTS IN COMBINATION WITH OTHER PRODUCTS IN A MANNER NOT EVALUATED OR CONTEMPLATED BY NATIONAL INSTRUMENTS, THE USER OR APPLICATION DESIGNER IS ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY OF NATIONAL INSTRUMENTS PRODUCTS WHENEVER NATIONAL INSTRUMENTS PRODUCTS ARE INCORPORATED IN A SYSTEM OR APPLICATION, INCLUDING, WITHOUT LIMITATION, THE APPROPRIATE DESIGN, PROCESS AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

Compliance

FCC/Canada Radio Frequency Interference Compliance*

Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC Web site at `fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the FCC and the Canadian DOC.

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information** pertaining to the CE Mark compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

Conventions

The following conventions are used in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.When this symbol is marked on the product, see the *Safety Information* section for precautions to take.
1394	Refers to a high-speed external bus that implements the IEEE 1394 serial bus protocol.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
Macintosh	Macintosh refers to all Macintosh computers with PCI bus, unless otherwise noted.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
PC	Refers to the IBM PC/XT, IBM PC/AT, and compatible computers.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ devices.

Abbreviations, acronyms, definitions, metric prefixes, mnemonics, and symbols are listed in the *Glossary*.

Contents

Chapter 1
Introduction

Chapter 2
Installing and Configuring the Device

Chapter 3
Hardware Overview

Chapter 4
Signal Connections

1 Introduction

The National Instruments DAQPad-6070E is a high-performance multifunction analog, digital, and timing I/O device for computers with IEEE 1394 ports. Supported functions include analog input (AI), analog output (AO), digital I/O (DIO), and timing I/O (TIO).

This chapter describes the DAQPad-6070E, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack the DAQPad-6070E.

The following documents contain information you may find helpful:

- *DAQ-STC Technical Reference Manual,* located at `ni.com/manuals`
- The NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, located at `ni.com/zone`

About the DAQPad-6070E

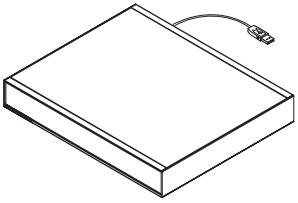
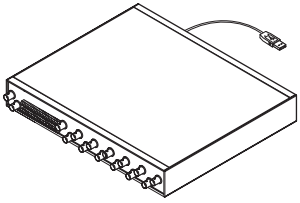
Thank you for buying a DAQPad-6070E. This product has the following features:

- A 12-bit A/D converter (ADC) with 16 analog inputs
- Two 12-bit D/A converters (DACs) with two voltage outputs
- Eight lines of transistor-transistor logic (TTL)-compatible DIO
- Two 24-bit counter/timers for TIO

Because the DAQPad-6070E does not have DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

There are two versions of the DAQPad-6070E: the DAQPad-6070E with a 68-pin SCSI male I/O connector and the DAQPad-6070E with BNC and removable screw terminal connectors. Table 1-1 illustrates the different I/O connectivity and form factors of each version.

Table 1-1. DAQPad-6070E Models

DAQ Device	I/O Connector
DAQPad-6070E 	68-pin SCSI II Male
DAQPad-6070E for BNC 	BNC and removable screw terminals

The DAQPad-6070E is a switchless, jumperless, hot-pluggable data acquisition (DAQ) device for 1394. 1394 automatically handles the assignment of all host resources, so you can install the device without powering off the computer. You can connect up to 64 DAQ devices to a single computer using 1394, although you will run out of bus bandwidth if all devices operate at full rate. In addition, the DAQPad-6070E provides up to 250 V of DC functional isolation from the PC.

The DAQPad-6070E uses the National Instruments DAQ-STC system timing controller for time-related functions. DAQ-STC consists of three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and have a maximum timing resolution of 50 ns. DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamless sampling rate change.

The DAQPad-6070E uses the Real-Time System Integration (RTSI) bus to easily synchronize multiple measurement functions to a common trigger or timing event. The RTSI bus consists of an RTSI bus interface and a shielded cable to route timing and trigger signals between several functions on as many as four DAQPads.

To control the DAQPad-6070E, use an SCXI system as the instrumentation front end. The DAQPad-6070E interface to an SCXI system allows the acquisition of more than 3,000 analog signals from thermocouples, resistance-temperature detectors (RTDs), strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control.

Detailed specifications for the DAQPad-6070E are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use the DAQPad-6070E, you need the following items:

- ❑ A computer
- ❑ DAQPad-6070E
- ❑ *DAQPad-6070E User Manual*
- ❑ NI-DAQ

Note Microsoft and NI do not support Windows 95 used with 1394, but Microsoft and NI do support Windows 2000/Me/98 with 1394. However, the connection through FireWire (1394) is only supported on single processor systems. If you are using a dual-processor computer, you must disable one of the processors.

- ❑ Optional: One of the following software packages and documentation:
  - LabVIEW
  - Measurement Studio
  - VI Logger

Unpacking

The DAQPad-6070E is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into your computer.

Store the DAQPad-6070E in the antistatic envelope when not in use.

Software Programming Choices

When programming the National Instruments DAQ hardware, you can use NI application development environment (ADE) software or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which shipped with the DAQPad-6070E, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the DAQPad-6070E.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you use LabVIEW, Measurement Studio, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

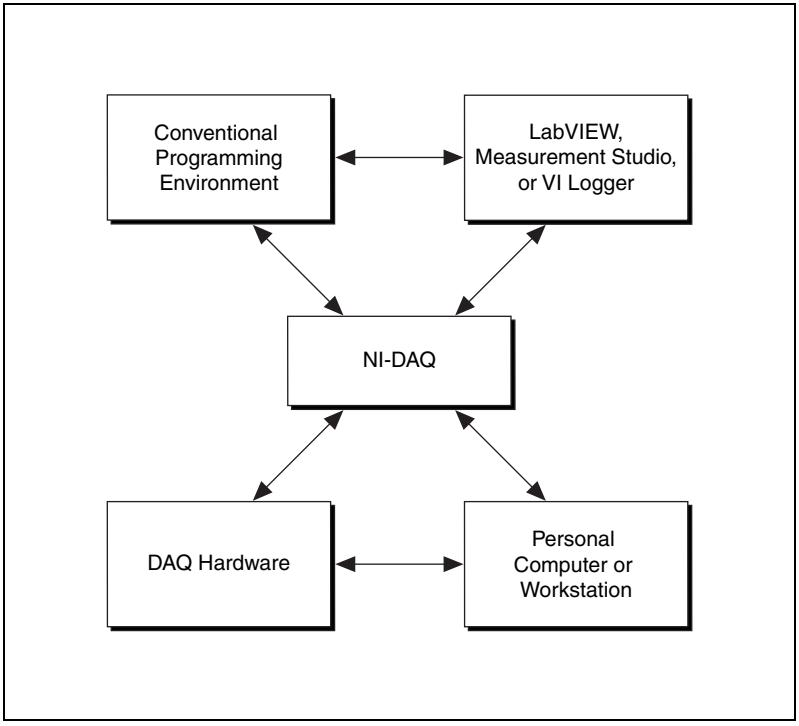


Figure 1-1. The Relationship Between the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design your test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National

Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

VI Logger is an easy-to-use yet flexible tool specifically designed for data logging applications. Using dialog windows, you can configure data logging tasks to easily acquire, log, view, and share your data. VI Logger does not require any programming; it is a stand-alone, configuration-based software.

Using LabVIEW, Measurement Studio, or VI Logger greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the DAQPad-6070E, including the following items:

- Cables and cable assemblies, shielded and ribbon
- BP-1 battery packs and chargers
- RTSI bus cables
- External expansion cables to connect to the external expansion connector located on the back panel of the DAQPad-6070E. This cable allows you to connect to SCXI in serial mode
- Low-channel count-signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more information about these products, refer to `ni.com`.

Custom Cabling

NI offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the differential AI signals, shielded twisted-pair wires for each AI pair yield the best results. Tie the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.
- Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

The parts in the following list are recommended for connectors that mate to the I/O connector on the DAQPad-6070E:

- Honda 68-position, solder cup, female connector
- Honda backshell

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. Operate the product only at or below the pollution degree stated in Appendix A, *Specifications*. Pollution is foreign

matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

Clean the product with a soft nonmetallic brush. Make sure that the product is completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate this product only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire board (PWB) on the secondary of an isolation transformer.

  Examples of installation category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

  Examples of installation category II are measurements on household appliances, portable tools, and similar equipment.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

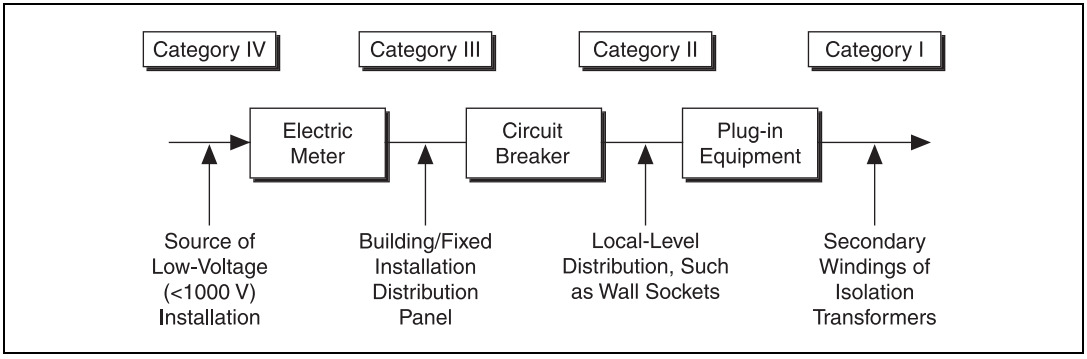
- Installation category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

  Examples of installation category III include measurements on distribution circuits and circuit breakers. Other examples of installation category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

Below is a diagram of a sample installation.



2

Installing and Configuring the Device

This chapter describes how to install and configure the DAQPad-6070E.

Installing the Software

Install the software before you install the DAQPad-6070E. Complete the following steps in order to complete the software installation:

1. Install the ADE, such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* that is included with the device.

Note It is important to install NI-DAQ before installing the DAQPad-6070E to ensure that the device is properly detected.

Installing the Hardware

You can connect the DAQPad-6070E to any available 1394 port. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

The DAQPad-6070E is equipped with two LEDs to help you determine the state of the device:

- Power LED
  - Off—No power is being provided to the device. Either the power cord is unplugged, or the power source is broken.
  - Dim—The device is receiving power but is not connected to an active 1394 port.
  - On—The device is receiving power and is connected to an active 1394 port.

- Communication LED—The COM LED blinks whenever the device sends or receives any commands or data. This LED should blink once when you first plug in the device. When you transfer large amounts of data, this light should be lit or continuously blinking.

Note If you are *not* using the BP-1 battery pack, follow the instructions below. If you are using the BP-1 battery pack, follow the installation instructions in the *BP-1 Battery Pack Installation Guide* and disregard step 1 below.

1. Connect the power cord to the wall outlet and the DAQPad-6070E.
2. Connect the 1394 cable from the computer or any other 1394 device to either port on the DAQPad-6070E. The computer should immediately detect the DAQPad-6070E. When the computer recognizes the device, the COM LED on the front panel will blink. Refer to the *Installing the Hardware* section for information on LEDs.
3. The power LED should be on.
4. Configure the DAQPad-6070E and any accessories with NI-DAQ.

Note Since the DAQPad-6070E is a software-configurable, Plug and Play instrument, the Plug and Play services query the instrument and allocate the required resources. The operating system enables the instrument for operation. Refer to the software documentation for more information.

The DAQPad-6070E is now installed.

3

Hardware Overview

This chapter presents an overview of the hardware functions on the DAQPad-6070E. Figure 3-1 shows the block diagram for the DAQPad-6070E.

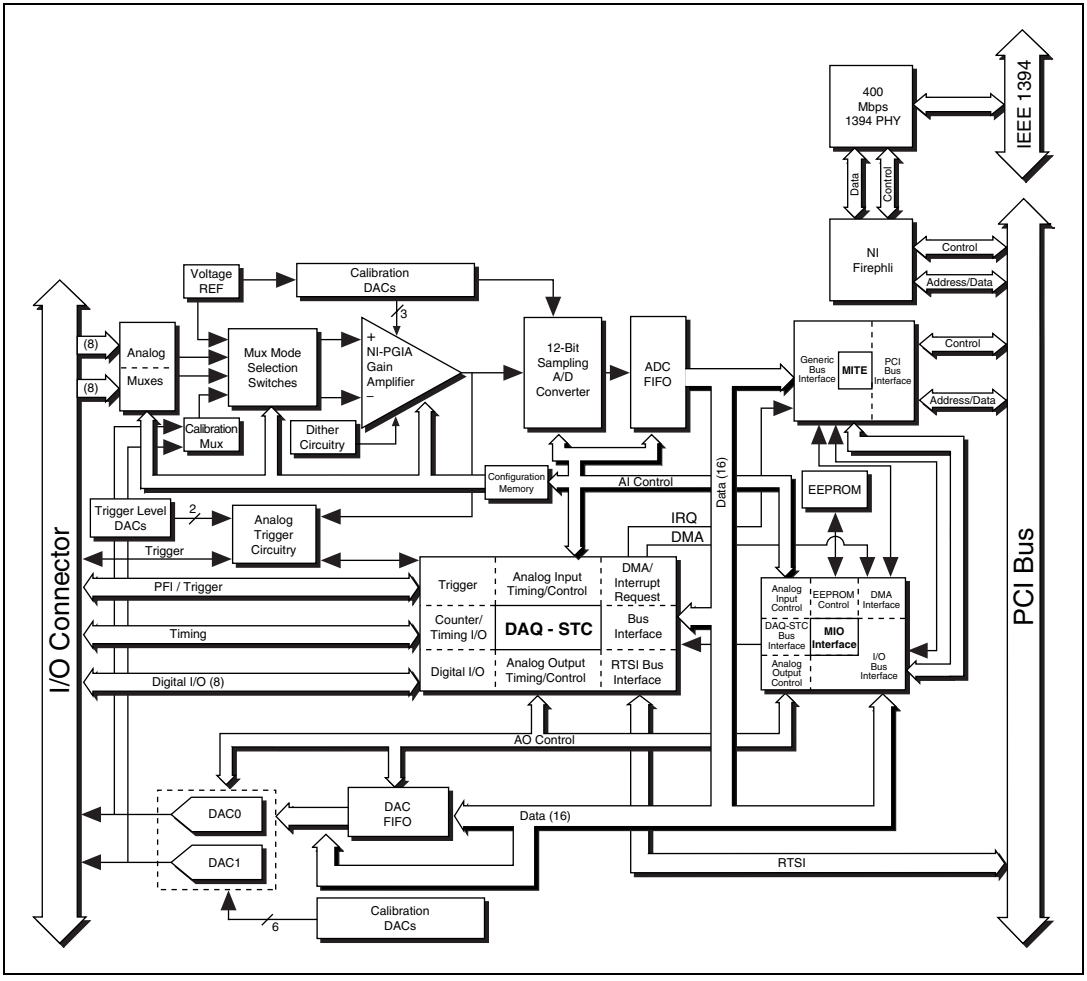


Figure 3-1. DAQPad-6070E Block Diagram

Analog Input

The AI section of the DAQPad-6070E is software configurable. You can select different AI configurations through application software designed to control the DAQPad-6070E. The following sections describe in detail each AI category.

Input Mode

The DAQPad-6070E has three input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input modes, NRSE and RSE, provide up to 16 channels. The DIFF input mode provides up to eight channels. Input modes are programmed on a per channel basis for multiple-mode channel scanning. For example, you can configure the circuitry to scan 12 channels—four differentially-configured channels and eight single-ended channels. Table 3-1 describes the three input modes.

Table 3-1. Available Input Modes for the DAQPad-6070E

Mode	Description
DIFF	A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the analog input sense (AISENSE) input.

For more information about input modes, refer to the *Input Configurations* section in Chapter 4, *Signal Connections*, which contains diagrams showing the signal paths for the three modes.

Input Polarity and Input Range

The DAQPad-6070E has two input polarity settings—unipolar and bipolar. Unipolar input polarity means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input polarity means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The DAQPad-6070E has a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V). You can program polarity and range settings on a per channel basis so that you can uniquely configure each input channel.

The software-programmable gain on the DAQPad-6070E increases its flexibility by matching the input signal ranges to those that the ADC can accommodate. The device has gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and is suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Precision[1]
0 to +10 V	1.0	0 to +10 V	2.44 mV
	2.0	0 to +5 V	1.22 mV
	5.0	0 to +2 V	488.28 µV
	10.0	0 to +1 V	244.14 µV
	20.0	0 to +500 mV	122.07 µV
	50.0	0 to +200 mV	48.83 µV
	100.0	0 to +100 mV	24.41 µV
–5 to +5 V	0.5	–10 to +10 V	4.88 mV
	1.0	–5 to +5 V	2.44 mV
	2.0	–2.5 to +2.5 V	1.22 mV
	5.0	–1 to +1 V	488.28 µV
	10.0	–500 to +500 mV	244.14 µV
	20.0	–250 to +250 mV	122.07 µV
	50.0	–100 to +100 mV	48.83 µV
	100.0	–50 to +50 mV	24.41 µV

[1] The value of 1 least significant bit (LSB) of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

You should select the input polarity and range setting based on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal. For example, if the input signal will not be negative (below 0 V), unipolar input polarity is best. However, if the signal is zero or negative, unipolar input polarity will produce inaccurate readings.

Dither

You control the dither circuitry with software. When you enable dither, you add approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging, such as calibration or spectral analysis, because it increases the resolution of the DAQPad-6070E. In such applications, noise modulation is decreased and differential linearity is improved by adding dither. When taking DC measurements, such as when checking the device calibration, you should enable dither and average at least 1,000 points to take a single reading. This process removes the effects of quantization and reduces noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you may want to disable the dither to reduce noise.

Figure 3-2 illustrates how dither affects signal acquisition. Figure 3-2a shows a small (±4 LSB) sine wave acquired with dither off. The ADC quantization is clearly visible. Figure 3-2b shows that when 50 such acquisitions are averaged together with dither off, quantization is still plainly visible. In Figure 3-2c, the sine wave is acquired with dither on, and there is a considerable amount of visible noise. But averaging about 50 such acquisitions with dither on, as shown in Figure 3-2d, eliminates both the added noise and the effects of quantization. Dither forces quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

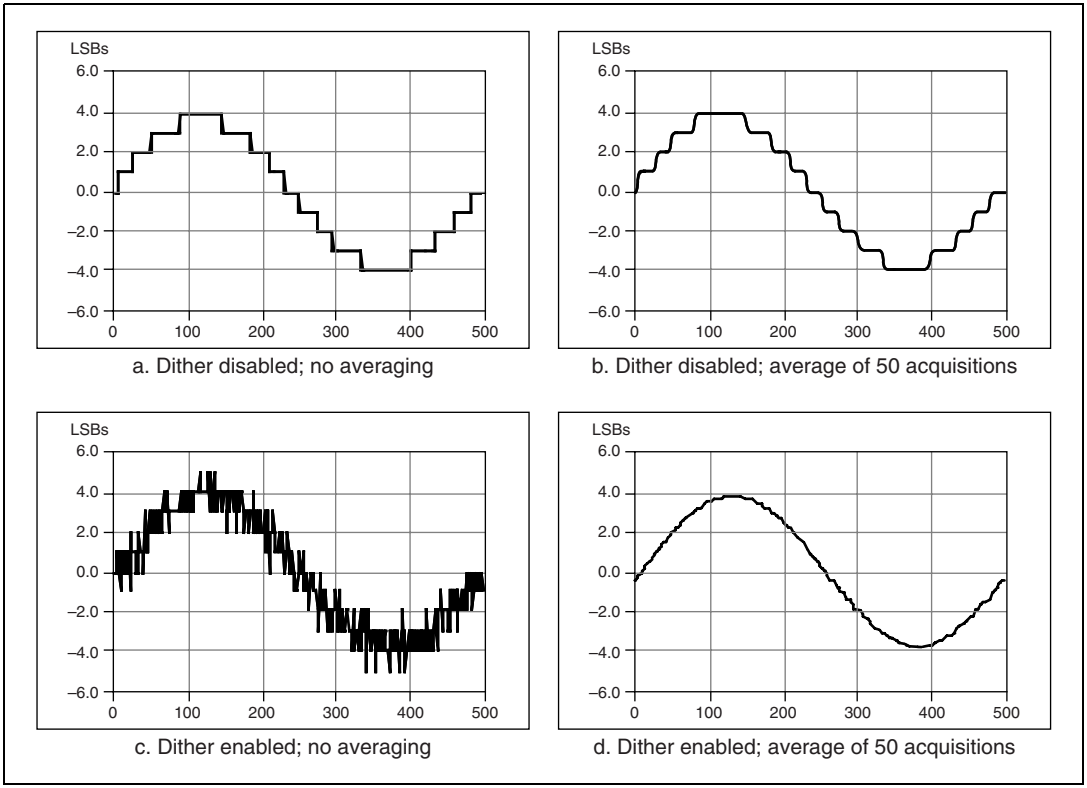


Figure 3-2. Dither and Signal Acquisition

Multiple Channel Scanning Considerations

The DAQPad-6070E can sample multiple channels at the same maximum rate as their single-channel rate; however, pay careful attention to the *settling time* for each device. Settling time is the time required for an amplifier, relays, or other circuits to reach a stable mode of operation. In the context of signal acquisition, the settling time for full-scale step is the amount of time required for a signal to reach a certain accuracy and stay within that accuracy range.

The settling time of the DAQPad-6070E is dependent, which can affect the useful sampling rate for a given gain. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for the DAQPad-6070E.

When scanning among channels at various gains, the settling times may increase. When the programmable gain instrumentation amplifier (PGIA) switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of 1 to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 16-bit device to settle within 0.0015% (15 ppm or 1 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. It may take as long as 200 µs for the circuitry to settle this much. In general, this extra settling time is unnecessary when the PGIA is switching to a lower gain.

Settling times can increase when scanning high-impedance signals because of a phenomenon called *charge injection*, where the AI multiplexer injects a small charge into each signal source when that source is selected. If the source impedance is too high, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ for high-speed scanning.

Because of the previously described limitations of settling times resulting from these conditions, multiple-channel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals nearly simultaneously. Data independently acquired from each channel (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on) is more accurate.

Analog Output

The DAQPad-6070E supplies two channels of AO voltage at the I/O connector. The reference and range for the AO circuitry is software-selectable. The reference can be either internal or external, and the range can be either bipolar or unipolar.

Analog Output Reference Selection

You can connect each DAC to the DAQPad-6070E internal reference of 10 V or to the external reference signal connected to the external reference (EXTREF) pin on the I/O connector. The signal applied to EXTREF should

be within ±11 V. You do not need to configure both channels to use the same reference.

Analog Output Polarity Selection

You can configure each AO channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. V_{ref} can be either the +10 V onboard reference or an externally supplied reference within ±11 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that data written to that DAC are interpreted as two's complement format. In two's complement mode, data values written to the AO channel can be either positive or negative. If you select unipolar range, data are interpreted in straight binary format. In straight binary mode, data values written to the AO channel range must be positive.

Analog Output Reglitch Selection

In normal operation, a DAC output *glitches*, or produces extra charge, whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit does *not* eliminate the glitches; it only makes them more uniform in size. Reglitching is normally disabled at startup, and you can independently enable each channel for reglitching with the software.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering, the DAQPad-6070E also supports analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a post-gain signal from the output of the PGIA, as shown in Figure 3-3. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256.

Note The PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input through software.

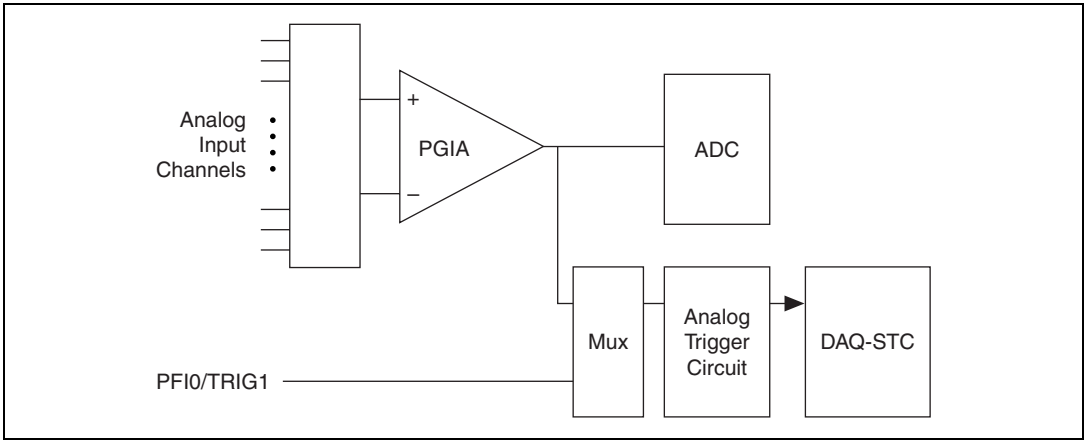


Figure 3-3. Analog Trigger Block Diagram

There are five analog triggering modes available, as shown in Figures 3-4 through 3-8. You can set **lowValue** and **highValue** independently with software.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is unused.

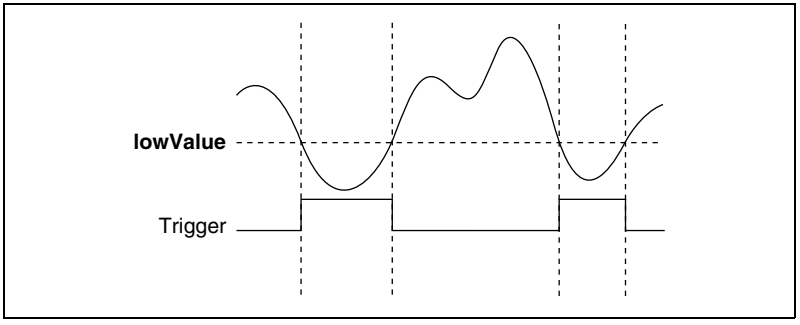


Figure 3-4. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is unused.

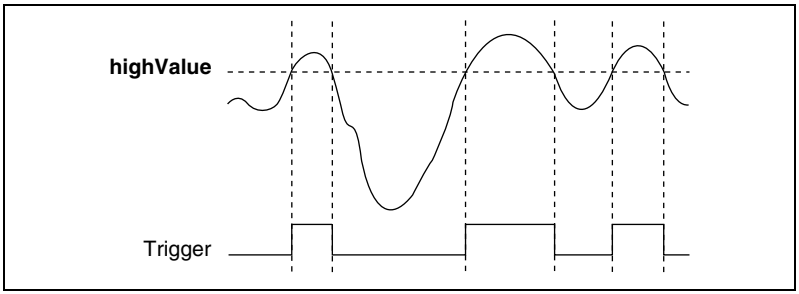


Figure 3-5. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between **lowValue** and **highValue**.

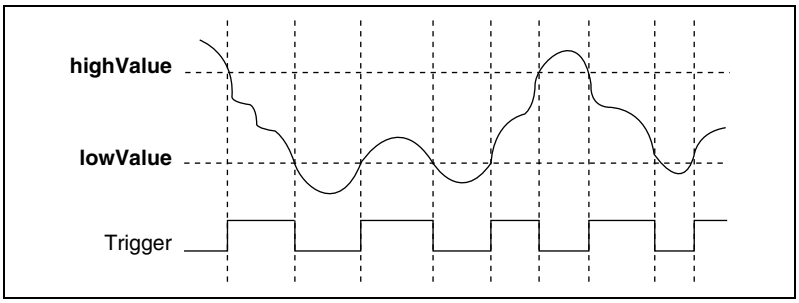


Figure 3-6. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**.

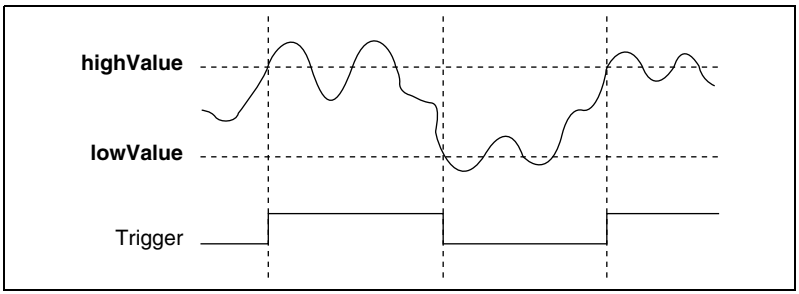


Figure 3-7. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**.

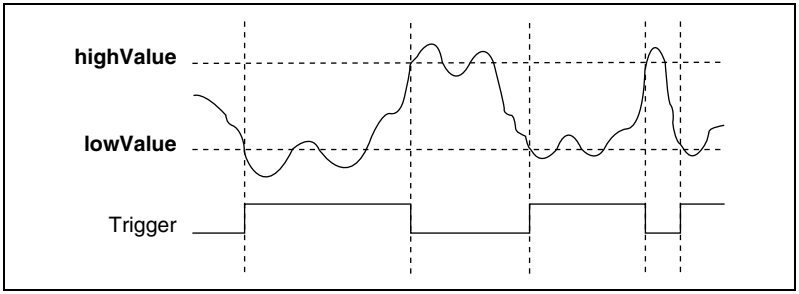


Figure 3-8. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the AI signal and the user-defined trigger levels. You can use this digital trigger through any DAQ-STC timing section, including the analog input, analog output, and general-purpose counter/timer sections. For example, you can configure the AI section to acquire *n* scans after the AI signal crosses a specific threshold. As another example, you can configure the AO section to update its outputs whenever the AI signal crosses a specific threshold.

Digital I/O

The DAQPad-6070E contains eight lines of DIO for general-purpose use. Each line is software configurable as either an input or an output. At system startup and reset, the DIO ports are all set to high-impedance.

The hardware up/down controls for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The DAQPad-6070E uses the RTSI bus to interconnect timing signals between devices, and the Programmable Function Input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the

DAQPad-6070E to both control and be controlled by other devices and circuits.

You can control 13 timing signals internal to DAQ-STC by an external source. These timing signals can also be controlled by signals internally generated to DAQ-STC, and these selections are fully software configurable. For example, the signal-routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-9.

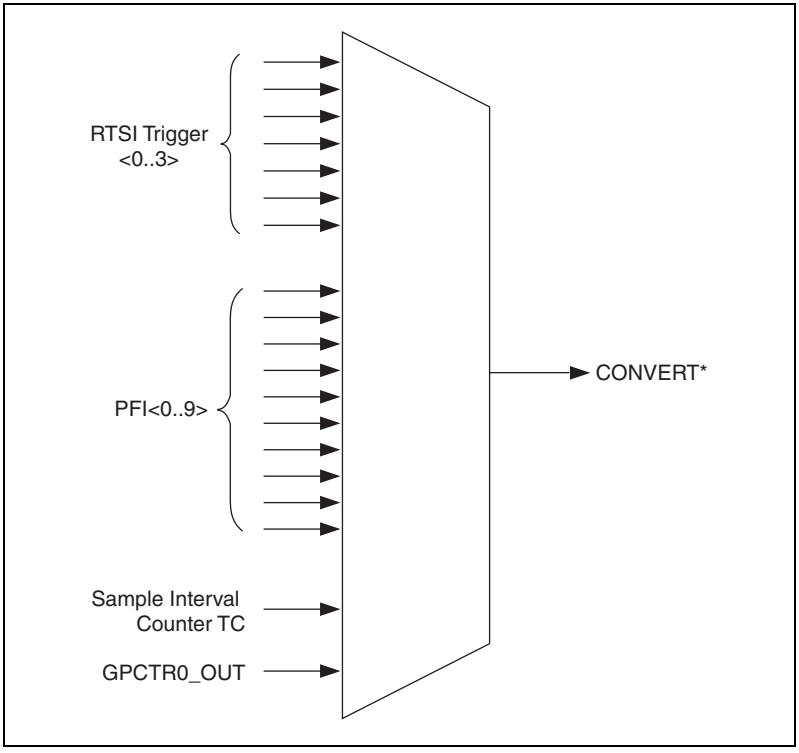


Figure 3-9. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..3> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section, and on the PFI pins, as indicated in the *Programmable Function Inputs* section in Chapter 4, *Signal Connections*.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and you can use software to select a PFI as the external source for a given timing signal. Any PFI can be used as an input by any timing signal and that multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each PFI pin to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, the software can start the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many functions performed by the DAQPad-6070E require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

You can program the DAQPad-6070E to use either its internal 20 MHz timebase or a timebase received over the RTSI bus on the RTSI clock line. If you configure the device to use the internal timebase, you can program the device to drive the internal timebase over the RTSI bus to another device programmed to receive this timebase signal as the primary frequency source. The default configuration is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software-selectable.

RTSI Triggers

The four RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for any DAQPad-6070E sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-10.

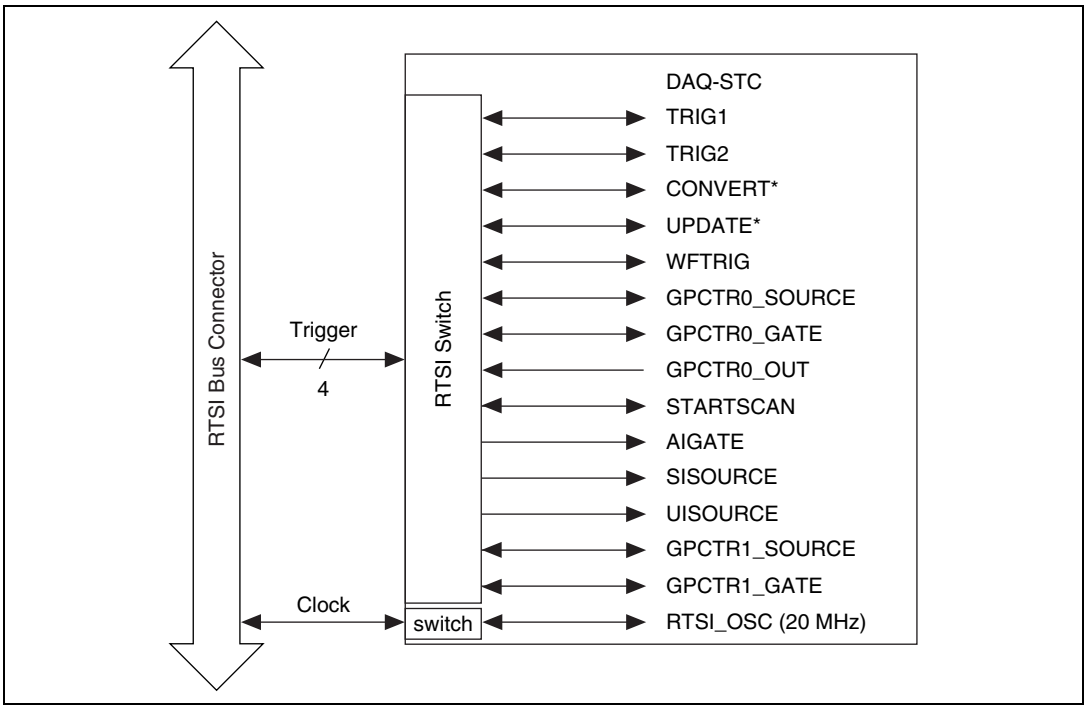


Figure 3-10. RTSI Bus Signal Connection

Refer to the *Timing Connections* section in Chapter 4, *Signal Connections*, for a description of the signals shown in Figure 3-10.

4

Signal Connections

This chapter describes how to make input and output signal connections to the DAQPad-6070E.

The DAQPad-6070E with BNCs provides easy-to-use, user I/O directly on the front of the box. Analog input, analog output, GPCTR0 Out, PFI0, and the external reference are accessible through BNCs. You can use USER1 and USER2 to convert a signal on a BNC cable to a signal wire on the connector block. This conversion makes connecting a BNC cable to a PFI/Trigger pin easier. The other signals are accessible through a removable screw terminal block. Extra removable terminal blocks are available.

The DAQPad-6070E with mass termination has a 68-pin connector that you can connect to a 68-pin accessory with the SH6868 shielded cable or the R6868 ribbon cable. With the SH6850 shielded cable or R6850 ribbon cable, you can connect the device to 50-pin signal conditioning modules and terminal blocks.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the DAQPad-6070E with mass termination. Figure 4-2 shows the pin assignments for the front panel I/O connections on the DAQPad-6070E with BNCs.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure 4-1. I/O Connector Pin Assignment for the DAQPad-6070E with Mass Termination

PFI 9	2	1	DIO 7
PFI 8	4	3	DIO 6
PFI 7	6	5	DIO 5
PFI 6	8	7	DIO 4
PFI 5	10	9	DIO 3
PFI 4	12	11	DIO 2
PFI 3	14	13	DIO 1
PFI 2	16	15	DIO 0
PFI 1	18	17	GPCTR 1_OUT
DGND	20	19	DGND
USER 2	22	21	USER 1
FREQ_OUT	24	23	SCANCLK
+5 V	26	25	EXTSTROBE
+5 V	28	27	AISENSE
DNGD	30	29	AIGND

Figure 4-2. I/O Connector Pin Assignment for the DAQPad-6070E with BNCs

Each analog input for the DAQPad-6070E with BNCs has a switch that you set based on whether the BNC is connected to a floating source (FS) or a grounded source (GS). Figure 4-3 shows how the FS setting connects the negative terminal of the differential input to ground through a 5 kΩ in parallel with 0.1 µF resistor. Set the switch to GS to allow both positive and negative terminals to float. If you are using a single-ended channel or using a differential channel connected to a grounded source, set the switch to GS. If you are using a differential channel connected to a floating source, set the switch to FS.

Refer to the *Measuring More than Eight Channels with the BNC Version of the DAQPad-6070E* section for more information on single-ended channels, differential channels, floating sources, and grounded sources.

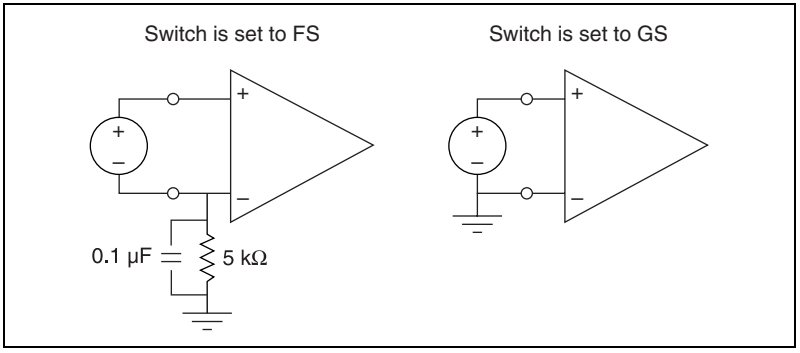


Figure 4-3. Floating Source and Grounded Source Connections

I/O Connector Signal Descriptions

The following table describes the types of input and output signals for the DAQPad-6070E.

Table 4-1. I/O Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on the DAQPad-6070E through separate, grounded planes.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This output supplies the voltage output of AO channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This output supplies the voltage output of AO channel 1.
EXTREF	A0GND	Input	External Reference—This input is the external reference input for the AO circuitry.
AOGND	—	—	Analog Output Ground—The AO voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on the DAQPad-6070E through separate grounded planes.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQPad-6070E through separate grounded planes.
DIO<0..7>	DGND	Input or Output	Digital I/O Signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.

Table 4-1. I/O Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
SCANCLK	DGND	Output	Scan Clock—This output pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input Output	PFI0/Trigger 1—As an input, this is either a PFI or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section. The hardware analog trigger is explained in the *Analog Trigger* section in Chapter 3, *Hardware Overview*. As an output, this pin is the TRIG1 signal. In posttrigger DAQ sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input Output	PFI1/Trigger 2—As an input, this is a PFI. As an output, this pin is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input Output	PFI2/Convert—As an input, this is a PFI. As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input Output	PFI3/Counter 1 Source—As an input, this is a PFI. As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input Output	PFI4/Counter 1 Gate—As an input, this is a PFI. As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.

Table 4-1. I/O Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is a PFI.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the AO primary group is being updated.
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG signal. In timed AO sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is a PFI.
		Output	As an output, this is the STARTSCAN signal. This signal pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is a PFI.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is a PFI.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-2. I/O Signal Summary for the DAQPad-6070E

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AISENSE, AISENSE2	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA

Table 4-2. I/O Signal Summary for the DAQPad-6070E (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
EXTREF	AI	10 kΩ	25/15	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	AI DIO	10 kΩ	±35 V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	9 kΩ pu and 10 kΩ pd
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input
AO = Analog Output
DIO = Digital Input/Output
DO = Digital Output
pu = pull up
AI/DIO = Analog/Digital Input/Output

Note: The tolerance on the 50 kΩ pull up and pull down resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two signal types.

Floating Signal Sources

A floating signal source is not connected to the building ground system and instead has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to the DAQPad-6070E AI ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground, so it is already connected to a common ground point with respect to the DAQPad-6070E, assuming the two are plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

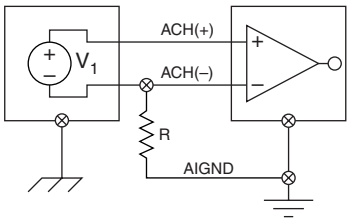
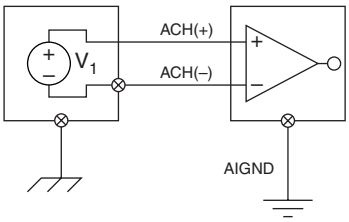
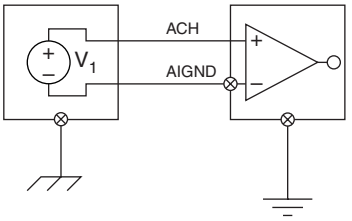
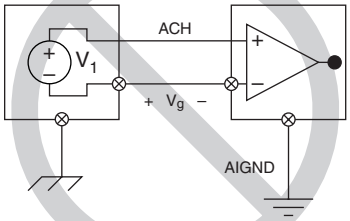
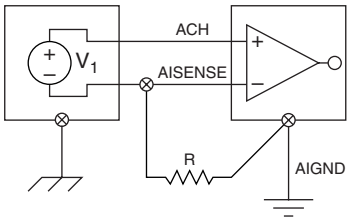
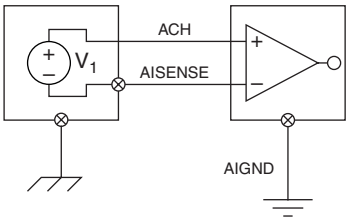
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are improperly connected. If a grounded signal source is improperly measured, this difference may appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Input Configurations

The following sections discuss using single-ended and differential measurements and the considerations for measuring both floating and ground-referenced signal sources.

Table 4-3 summarizes the recommended input configuration for both types of signal sources.

Table 4-3. Summary of Analog Input Connections

Input	Signal Source Type	
	Floating Signal Source (Not Connected to Building Ground)	**Grounded Signal Source**
	Examples • Ungrounded Thermocouples • Signal Conditioning with Isolated Outputs • Battery Devices	Examples • Plug-in Instruments with Nonisolated Outputs
Differential (DIFF)	 See text for information on bias resistors.	
Single-Ended — Ground Referenced (RSE)		NOT RECOMMENDED  Ground-loop losses, V_g, are added to measured signal.
Single-Ended — Nonreferenced (NRSE)	 See text for information on bias resistors.	

Differential Connections (DIFF Input Mode)

A differential connection is one in which the DAQPad-6070E AI signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for DIFF input, each signal uses two multiplexer inputs—one for the signal and one for its reference. Therefore, with a DIFF configuration for every channel, as many as eight AI channels are available.

In DIFF input mode, the AI channels are paired, with ACH<i> as the signal input and ACH<i+8> as the signal reference. For example, ACH0 is paired with ACH8, ACH1 is paired with ACH9, and so on.

Use DIFF input connections for channels that meet any of the following conditions:

- The input signal is low-level (less than 1 V).
- The leads connecting the signal to the DAQPad-6070E are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pickup and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Ground-Referenced Signal Sources in DIFF Mode

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on the DAQPad-6070E in DIFF input mode.

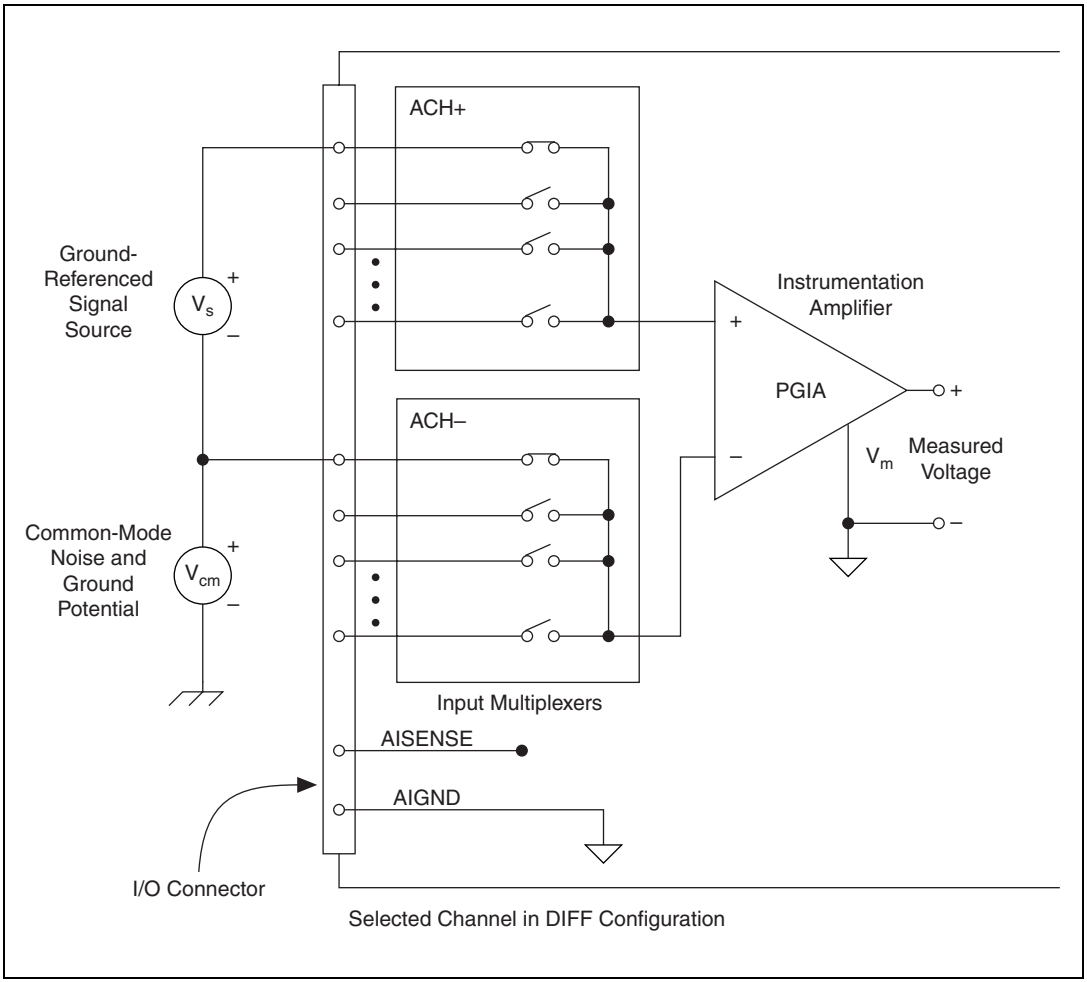


Figure 4-4. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the DAQPad-6070E ground, shown as V_{cm} in Figure 4-4.

Nonreferenced Signal Sources in DIFF Mode

Figure 4-5 shows how to connect a floating signal source to a channel on the DAQPad-6070E in DIFF input mode.

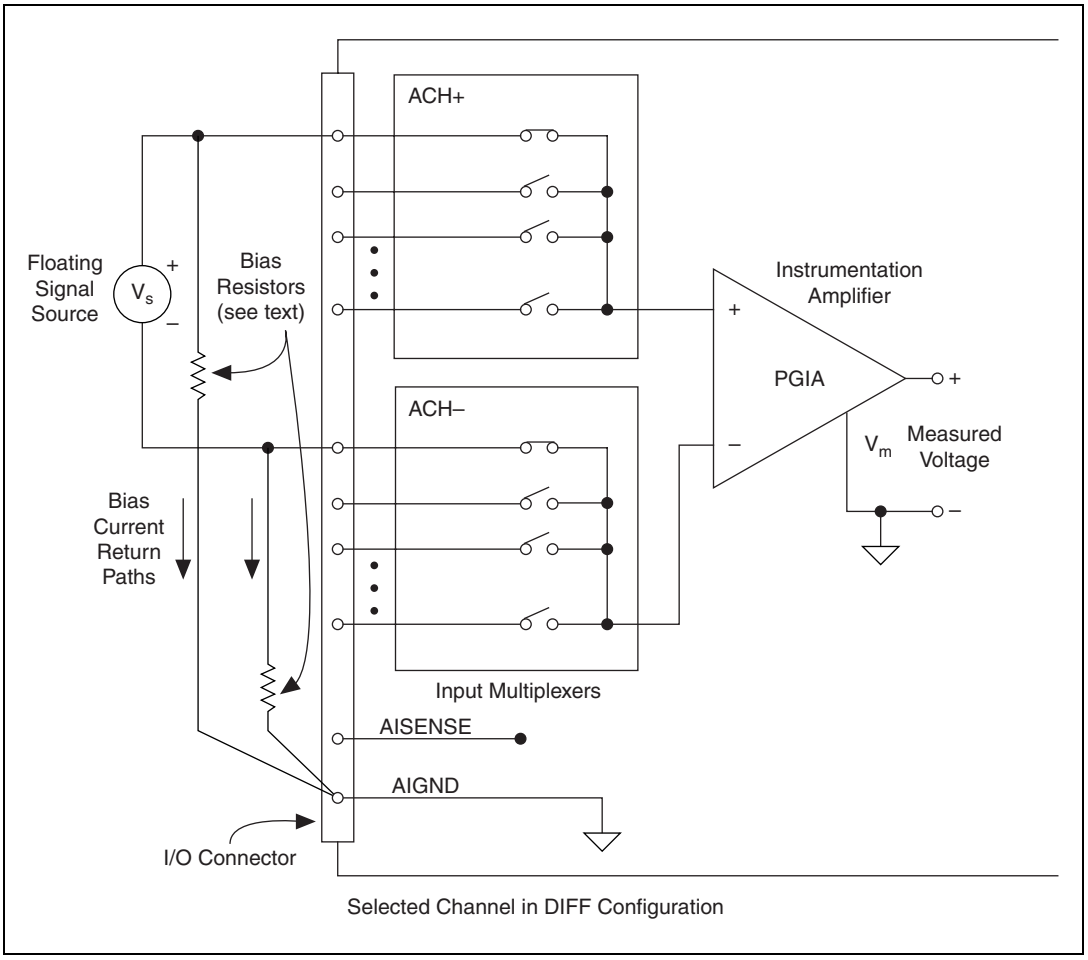


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is unlikely to remain within the common-mode signal range of the PGIA, and the PGIA saturates, causing erroneous readings. To prevent this problem, you must reference the source to AIGND. The easiest way to make this reference is to connect the positive side of the signal to the positive input of the PGIA and connect the negative

side of the signal to AIGND and to the negative input of the PGIA, without any resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor approximately 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance so that nearly equal amounts of noise couple onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high-input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described, using the same value resistor on both the positive and negative inputs; however, there is some gain error from loading down the source.

Single-Ended Connections

A single-ended connection is one in which the DAQPad-6070E AI signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel on the DAQPad-6070E with mass termination is configured for single-ended input, up to 16 AI channels are available. However, this feature is not available for the DAQPad-6070E with BNCs.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the DAQPad-6070E are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input configuration is recommended for signals that do not meet the preceding conditions.

You can configure the DAQPad-6070E channels with software for two types of single-ended connections—RSE input mode and NRSE input mode. Use RSE input mode for floating signal sources; in this case, the DAQPad-6070E provides the reference ground point for the external signal. Use NRSE input mode for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the DAQPad-6070E should not supply one.

In single-ended modes, more electrostatic and magnetic noise couples into the signal connections than in DIFF input mode. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Floating Signal Sources (RSE Input Mode)

Figure 4-6 shows how to connect a floating signal source to a channel on the DAQPad-6070E in RSE input mode.

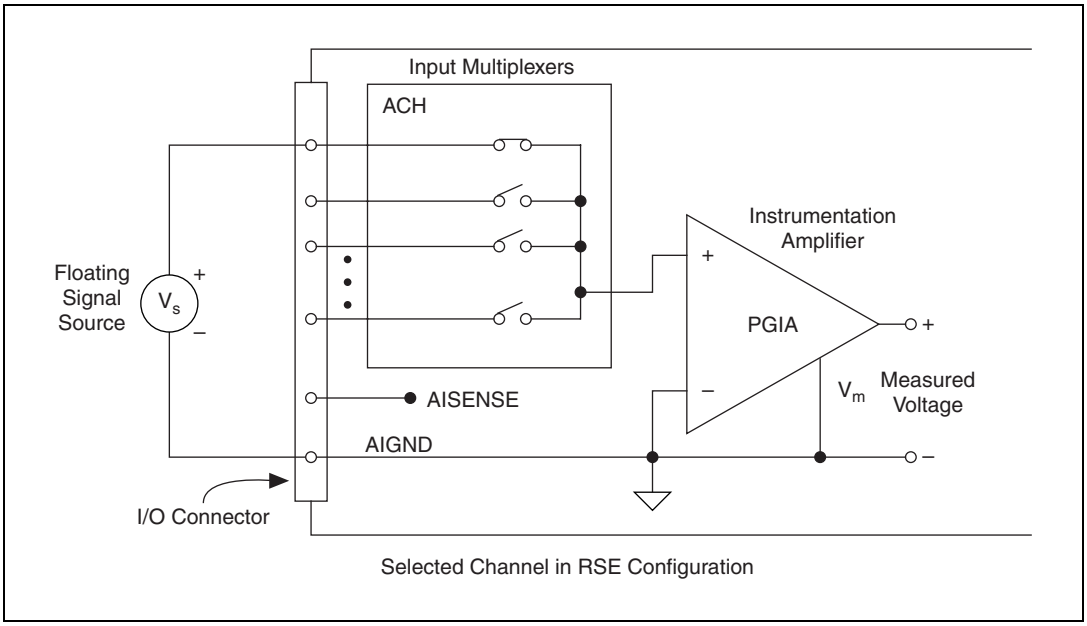


Figure 4-6. Single-Ended Input Connections for Nonreferenced or Floating Signals

Grounded Signal Sources (NRSE Input Mode)

To measure a grounded signal source with a single-ended mode, the DAQPad-6070E must be in NRSE input mode. Connect the signal to the positive input of the DAQPad-6070E PGIA, and the signal local ground reference to the PGIA negative input. Connect the signal ground point to the AISENSE pin. Any potential difference between the DAQPad-6070E ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA and is rejected by the amplifier. If the input circuitry of the DAQPad-6070E were referenced to ground similar to the RSE input mode, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-7 shows how to connect a grounded signal source to a channel on the DAQPad-6070E in NRSE input mode.

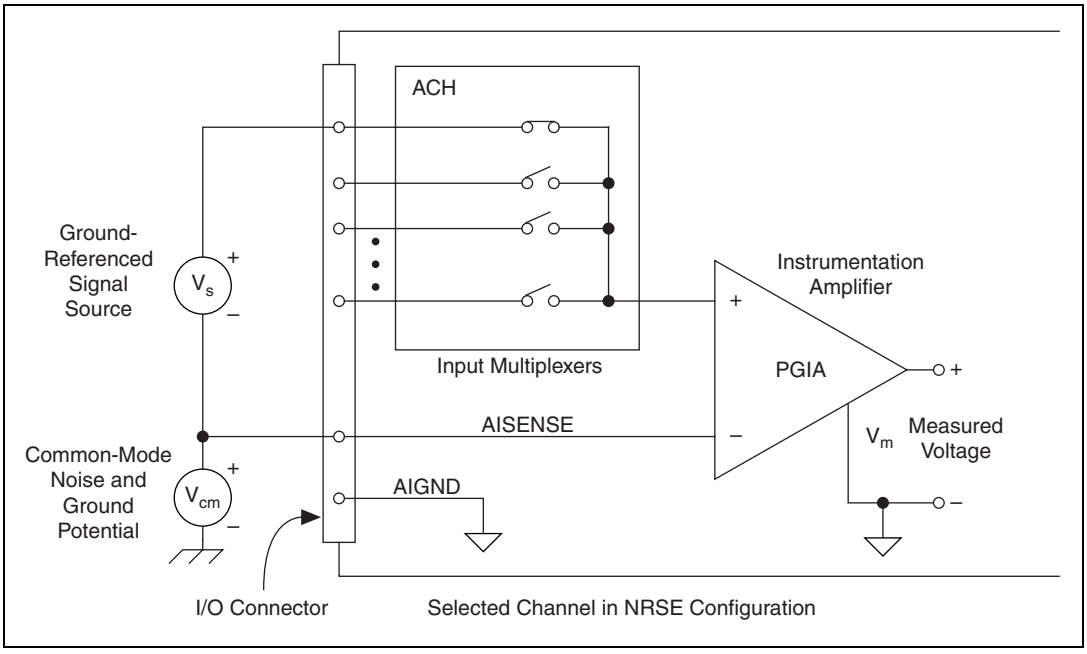


Figure 4-7. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-4 and 4-7 show connections for signal sources that are already referenced to some ground point with respect to the DAQPad-6070E. In these cases, the PGIA can reject voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as V^+_{in} and V^-_{in} (input signals) are both within ±11 V of AIGND.

Analog Input Signal Connections

The AI signals for the DAQPad-6070E are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are tied to the 16 AI channels of the DAQPad-6070E. In single-ended modes, signals connected to ACH<0..15> are routed to the positive input of the device PGIA. In DIFF mode, signals connected to ACH<0..7> are routed to the positive input of

the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

Caution Exceeding the differential or common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the DAQPad-6070E and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-2.

In NRSE input configuration, the AISENSE signal is internally connected to the negative input of the DAQPad-6070E PGIA when the corresponding channels are selected. In DIFF and RSE input configurations, this signal is not connected.

AIGND is an AI common signal that is routed directly to the ground tie point on the DAQPad-6070E. Use this signal for a general analog ground tie point to the DAQPad-6070E if necessary.

How you connect AI signals to the DAQPad-6070E depends on the configuration of the AI channels and the type of input signal source. With different configurations, you can use the PGIA in different ways. Figure 4-8 shows a diagram of the DAQPad-6070E PGIA.

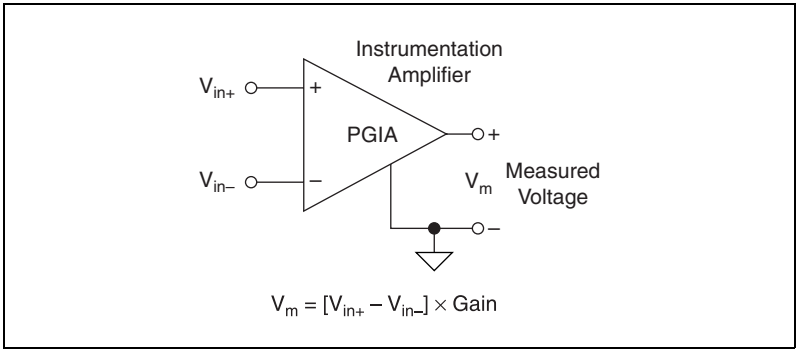


Figure 4-8. DAQPad-6070E PGIA

The PGIA applies gain and common-mode voltage rejection and presents high-input impedance to the AI signals connected to the DAQPad-6070E. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain of the amplifier. The amplifier output voltage is referenced to the

device ground. The DAQPad-6070E ADC measures this output voltage during A/D conversions.

Reference all signals to ground either at the source device or at the DAQPad-6070E. If you have a floating source, reference the signal to ground by using the RSE input configuration or the DIFF input configuration with bias resistors. For more information, refer to the *Nonreferenced Signal Sources in DIFF Mode* section. If you have a grounded source, do not reference the signal to AIGND. Instead, use DIFF or NRSE input configurations.

Measuring More than Eight Channels with the BNC Version of the DAQPad-6070E

The DAQPad-6070E for BNC measures up to eight differential channels using BNC connectors and cabling. To measure more than eight channels, use one of the single-ended measurements modes. Up to 16 single-ended channels are available in the single-ended measurement modes.

To use a single-ended measurement mode, change the source type (FS/GS) switch settings. Figure 4-9 shows the source type switch locations.

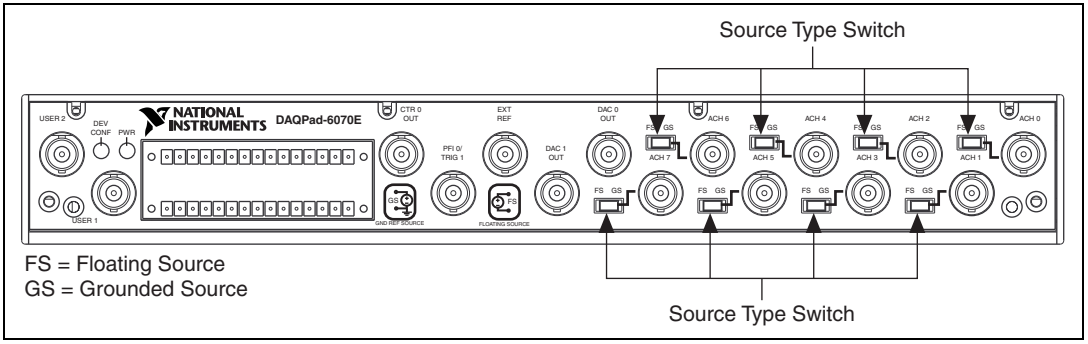


Figure 4-9. Front Panel of the DAQPad-6070E for BNC

For each BNC connector that you use for two channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure 4-10. When you set the source type to the GS position and software-configure the device for single-ended input, each BNC connector provides access to two single-ended channels, ACH(i) and ACH(i+8). For example, the BNC connector labeled ACH0 provides access to

single-ended channels ACH0 and ACH8, the BNC connector labeled ACH1 provides access to single-ended channels ACH1 and ACH9, and so on.

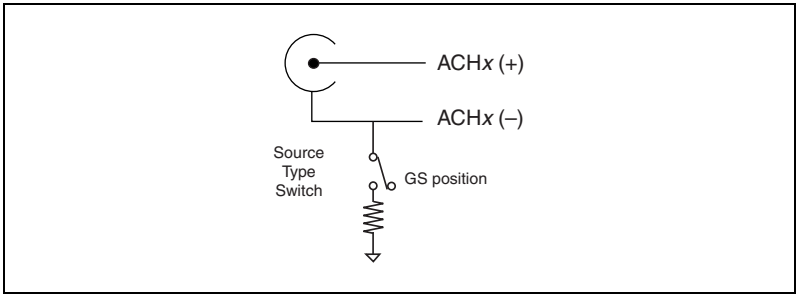


Figure 4-10. BNC Connector Wiring

Analog Output Signal Connections

The AO signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND. DAC0OUT is the voltage output signal for AO channel 0. DAC1OUT is the voltage output signal for AO channel 1.

EXTREF is the external reference input for both AO channels. Individually configure each AO channel for external reference to apply the signal at the external reference input for that channel. If you do not specify an external reference, the channel will use the internal reference. AO configuration options are explained in the *Analog Output* section in Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both AO channels and the external reference signal.

Figure 4-11 shows how to make AO connections and the external reference input connection to the DAQPad-6070E.

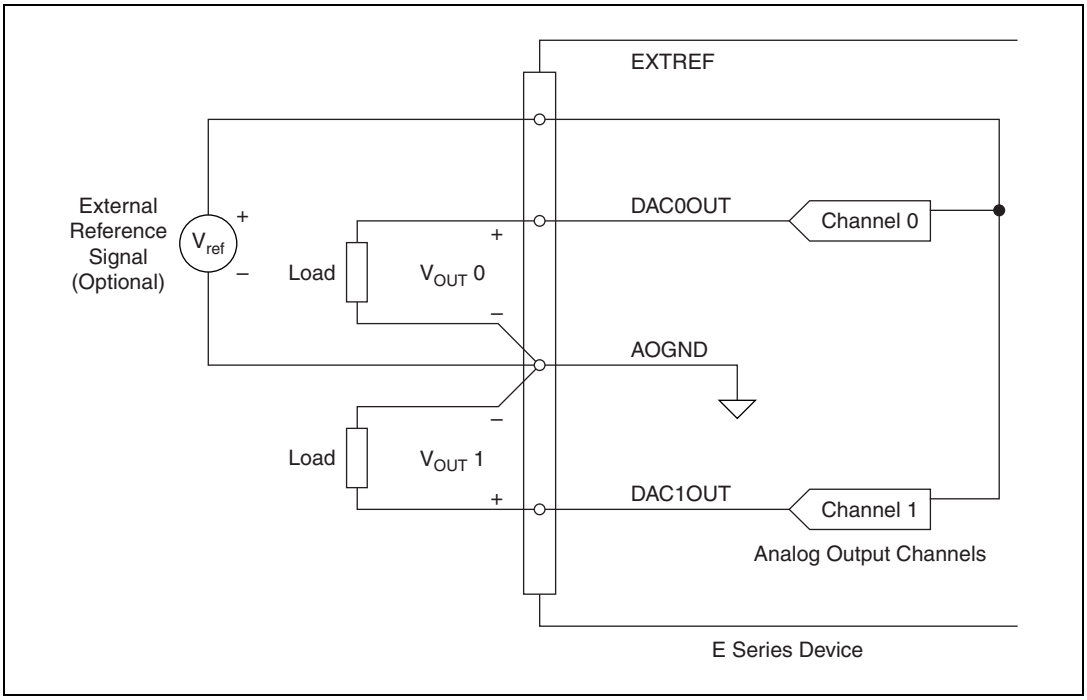


Figure 4-11. Analog Output Connections

The external reference signal can be either a DC or an AC signal. The device multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Digital I/O Signal Connections

The DIO signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program each line to be an input or an output.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the DAQPad-6070E and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-12 shows signal connections for three typical DIO applications.

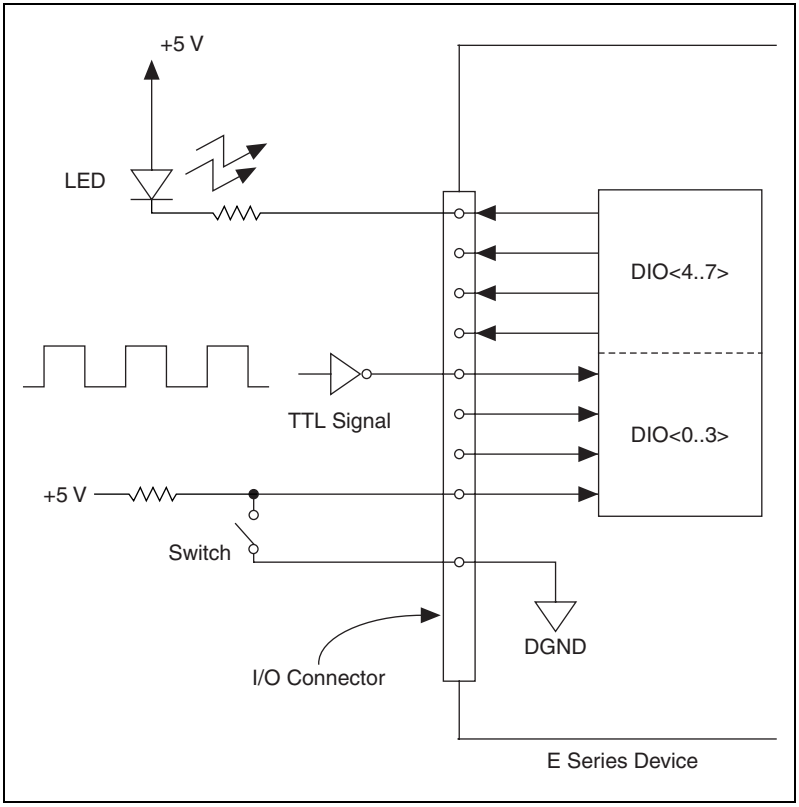


Figure 4-12. Digital I/O Connections

Figure 4-12 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the state of the switch in Figure 4-12. Digital output applications include sending TTL signals and driving external devices, such as the LED in Figure 4-12.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply through a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The power rating of the fuse is +4.65 to +5.25 VDC at 1 A.

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the DAQPad-6070E or any other device. Doing so can damage the DAQPad-6070E and the computer. NI is *not* liable for damage resulting from such a connection.

Timing Connections

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the DAQPad-6070E and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control over the DAQPad-6070E timing is routed through the 10 PFIs labeled PFI0 through PFI9. These signals are explained in detail in the *Programmable Function Input Connections* section. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform-generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform-generation, and general-purpose timing signals.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-13, which shows an external TRIG1 source and an external CONVERT* source connected to two PFI pins.

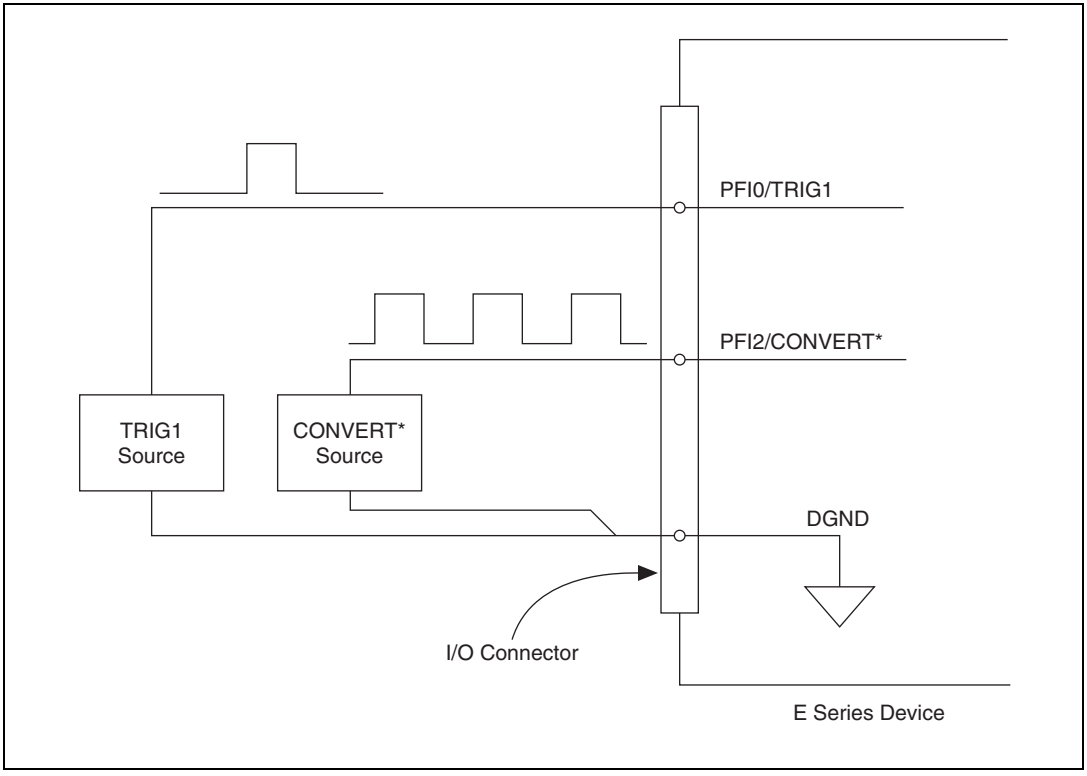


Figure 4-13. Timing I/O Connections

Programmable Function Input Connections

You can externally control 13 internal timing signals from the PFI pins. The source for each signal is software-selectable from any PFI. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for applications requiring alternative wiring.

You can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. However, do not externally drive a PFI signal when it is configured as an output.

As an input, you can individually configure each PFI for edge or level detection and for polarity selection. You can use the polarity selection for any timing signal, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed in the *Data Acquisition Timing Signals* section.

In edge-detection mode, the minimum pulse width required is 10 ns. This requirement applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs, but there may be limits imposed by the timing signal being controlled. These requirements are stated in the descriptions of the individual signals in the *Data Acquisition Timing Signals* section.

Data Acquisition Timing Signals

The timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

You can use posttriggered data acquisition to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ operation is shown in Figure 4-14. On the DAQPad-6070E, each STARTSCAN pulse initiates one CONVERT* pulse.

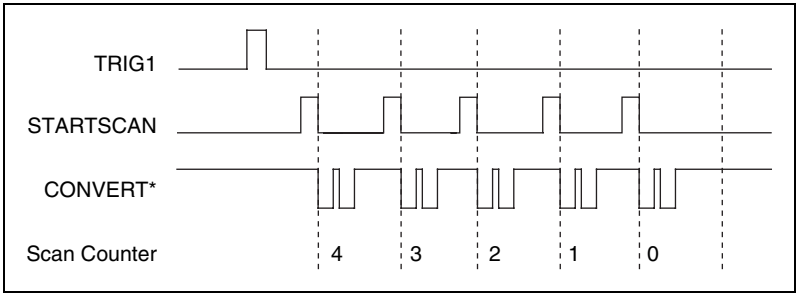


Figure 4-14. Typical Posttriggered Acquisition

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest, in addition to data acquired after the trigger. Figure 4-15 shows a typical pretriggered DAQ operation. Each signal shown in these figures is described later in this chapter.

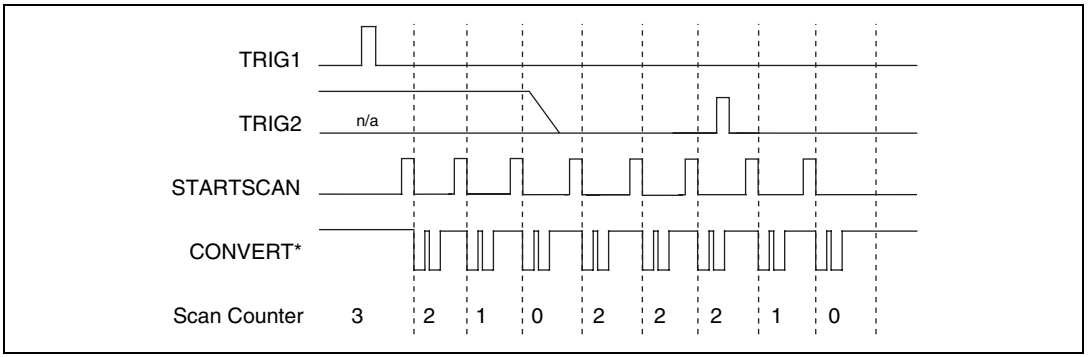


Figure 4-15. Typical Pretriggered Acquisition

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin. Refer to Figures 4-14 and 4-15 for the relationship of TRIG1 to the DAQ operation.

As an input, TRIG1 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG1 starts the DAQ sequence for both posttriggered and pretriggered acquisitions. The DAQPad-6070E supports analog triggering on the PFI0/TRIG1 pin. Refer to Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, TRIG1 reflects the action that initiates a DAQ operation, even if another PFI is externally triggering the acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-16 and 4-17 show the input and output timing requirements for TRIG1.

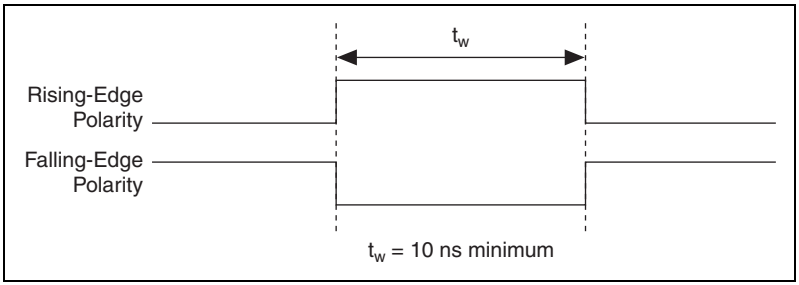


Figure 4-16. TRIG1 Input Signal Timing

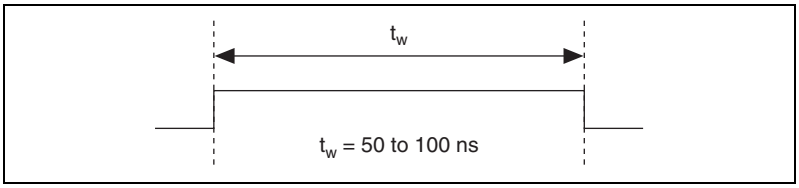


Figure 4-17. TRIG1 Output Signal Timing

The device also uses TRIG1 to initiate pretriggered operations. In most pretriggered applications, TRIG1 is generated by a software trigger, unless a pin is selected as the source of TRIG1. Refer to the *TRIG2 Signal* section for a complete description of the use of TRIG1 and TRIG2 in a pretriggered operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-15 for the relationship of TRIG2 to the sequence.

As an input, TRIG2 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG2 initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter (SC) indicates the minimum number of scans before TRIG2 can be recognized. After the SC decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores TRIG2 if it is asserted before the SC decrements to zero. After the selected edge of TRIG2 is received, the

device acquires a fixed number of scans, and the acquisition stops. This mode acquires data before and after receiving TRIG2.

As an output, TRIG2 reflects the posttrigger in a pretriggered acquisition sequence, even if the acquisition is being externally triggered by another PFI. TRIG2 is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-18 and 4-19 show the input and output timing requirements for TRIG2.

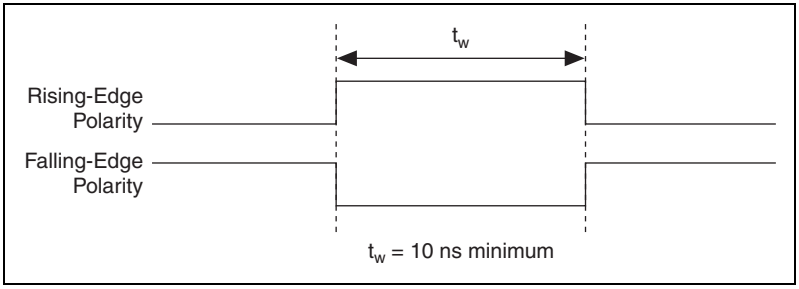


Figure 4-18. TRIG2 Input Signal Timing

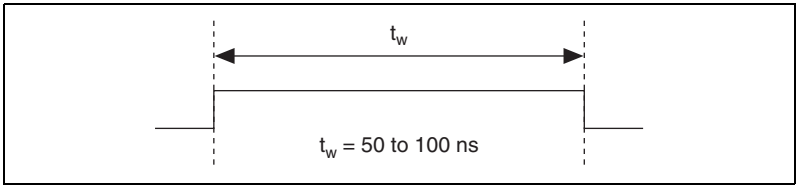


Figure 4-19. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can receive as an input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-14 and 4-15 for the relationship of STARTSCAN to the sequence.

As an input, STARTSCAN is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of STARTSCAN initiates a scan. The sample interval counter (SI2) starts if you select an internally triggered the CONVERT* signal.

As an output, STARTSCAN reflects the actual start pulse that initiates a scan, even if the starts are being externally triggered by another PFI. You have two output options: an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan, or an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN is deasserted t_{off} after the last conversion in the scan initiates. This output is set to high-impedance at startup.

Figures 4-20 and 4-21 show the input and output timing requirements for STARTSCAN.

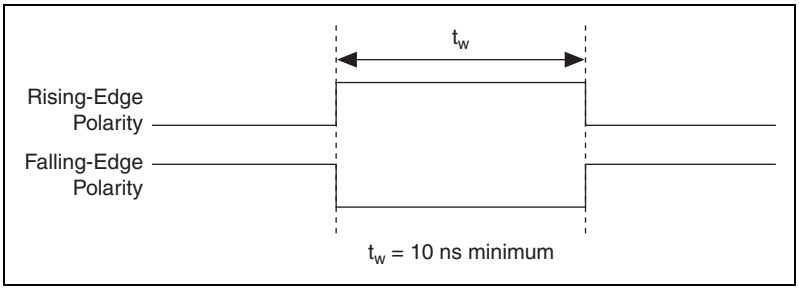


Figure 4-20. STARTSCAN Input Signal Timing

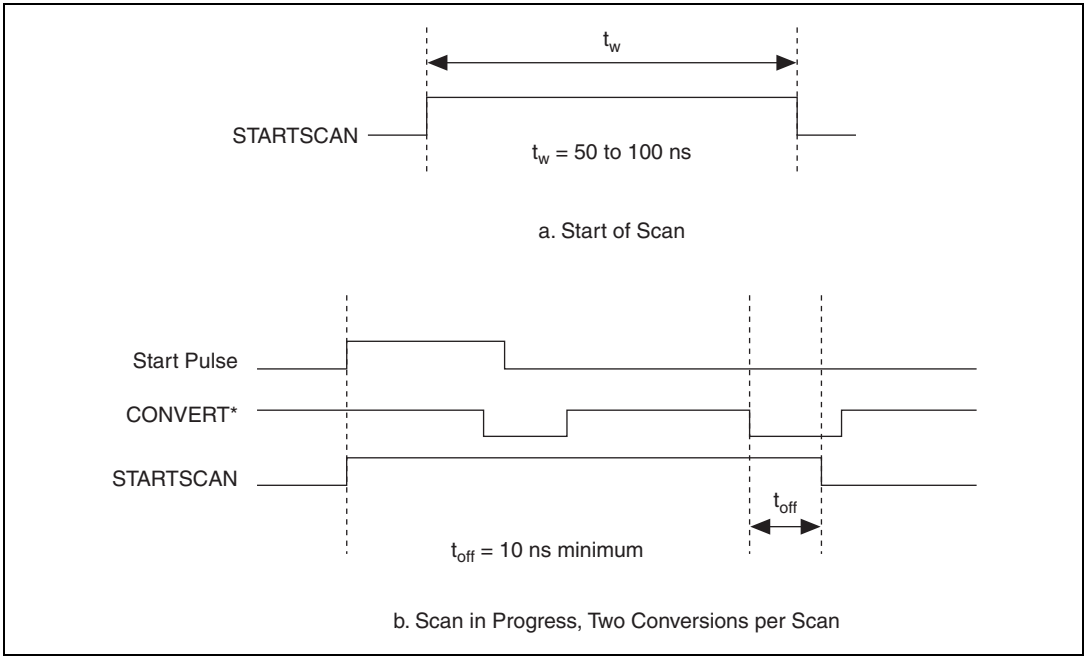


Figure 4-21. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates STARTSCAN. If you use internally generated conversions, the first CONVERT* appears when the onboard SI2 counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on the DAQPad-6070E internally generates STARTSCAN unless you select an external source. This counter is started by the TRIG1 signal and is stopped either by software or the SI2 counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a sequence. Scans occurring within a sequence may be gated by either the hardware AIGATE signal or the software command register gate.

CONVERT* Signal

Any PFI pin can receive as an input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-14 and 4-15 for the relationship of CONVERT to the sequence.

As an input, CONVERT* is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of CONVERT* initiates an A/D conversion.

As an output, CONVERT* reflects the actual convert pulse that is connected to the ADC, even if another PFI is externally generating the conversions. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-22 and 4-23 show the input and output timing requirements for CONVERT*.

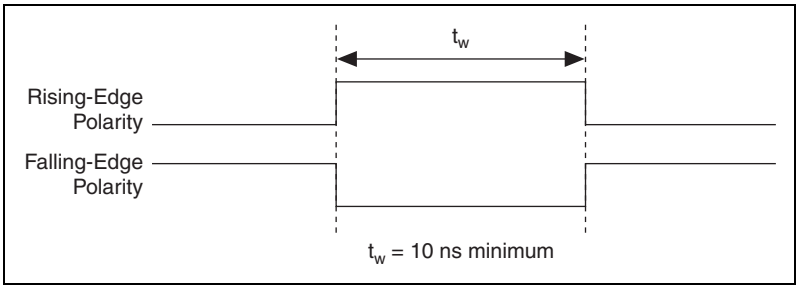


Figure 4-22. CONVERT* Input Signal Timing

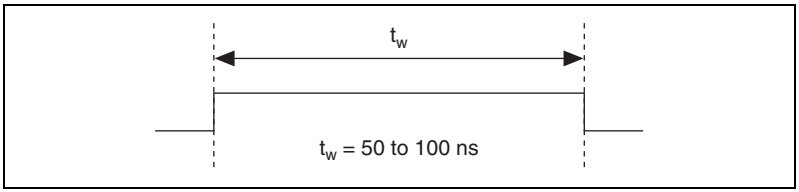


Figure 4-23. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. The hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The SI2 counter on the DAQPad-6070E generates CONVERT* unless you select an external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan finishes. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a sequence. Scans occurring within a DAQ sequence may be gated by either the hardware AIGATE signal or the software command register gate.

AIGATE Signal

Any PFI pin can receive as an input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or

edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode, if AIGATE is active, the STARTSCAN signal is masked off and no scans occur. In the edge-detection mode, the first active edge disables STARTSCAN, and the second active edge enables STARTSCAN.

AIGATE cannot stop a scan in progress or continue a previously gated-off scan. In other words, once a scan starts, AIGATE does not gate off conversions until the beginning of the next scan. Conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The SI2 counter uses SISOURCE as a clock to time the generation of the STARTSCAN signal. Configure the PFI pin you select as the source for SISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates SISOURCE unless you select an external source. Figure 4-24 shows the timing requirements for SISOURCE.

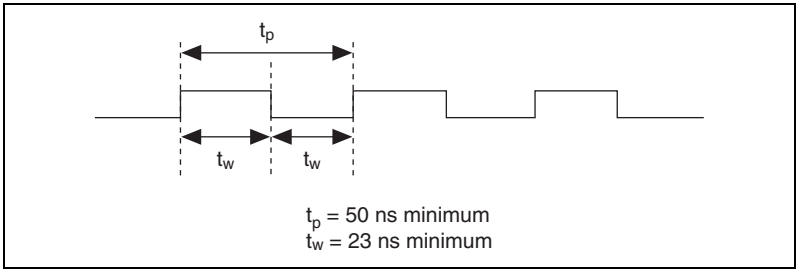


Figure 4-24. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins.

The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-25 shows the timing for SCANCLK.

Note The polarity of SCANCLK is not software-selectable when programmed using NI-DAQ. The polarity is set to a positive polarity pulse.

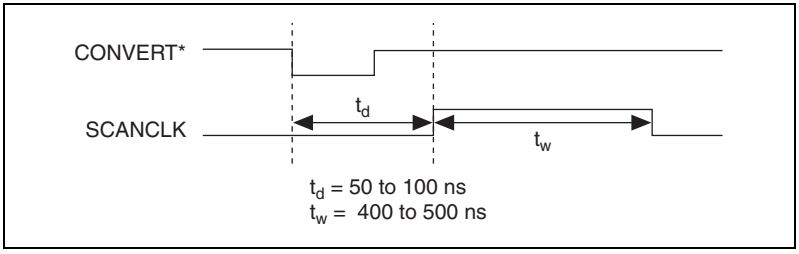


Figure 4-25. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of EXTSTROBE*. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode.

Note EXSTROBE* cannot be enabled using NI-DAQ.

Figure 4-26 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

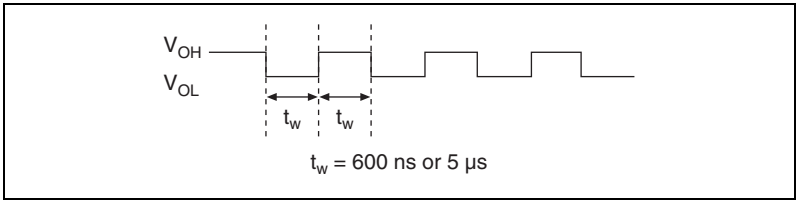


Figure 4-26. EXTSTROBE* Signal Timing

Waveform Generation Timing Connections

The analog group defined for the DAQPad-6070E is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin. As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. The update interval counter (UI) starts if you select the internally generated UPDATE* signal.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if the waveform generation is externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-27 and 4-28 show the input and output timing requirements for WFTRIG.

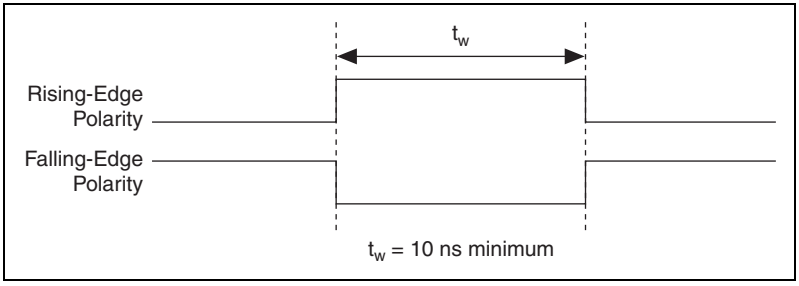


Figure 4-27. WFTRIG Input Signal Timing

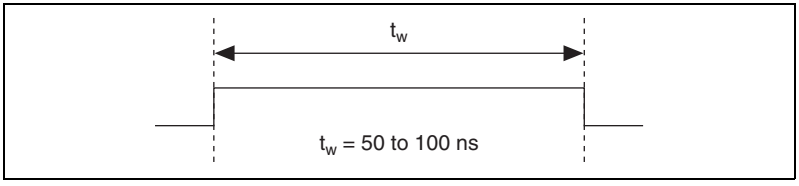


Figure 4-28. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin. As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. In order to use UPDATE*, set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse that is connected to the DACs, even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to high-impedance at startup.

Figures 4-29 and 4-30 show the input and output timing requirements for UPDATE*.

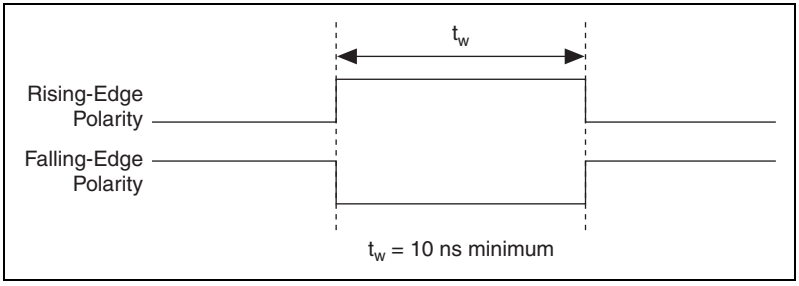


Figure 4-29. UPDATE* Input Signal Timing

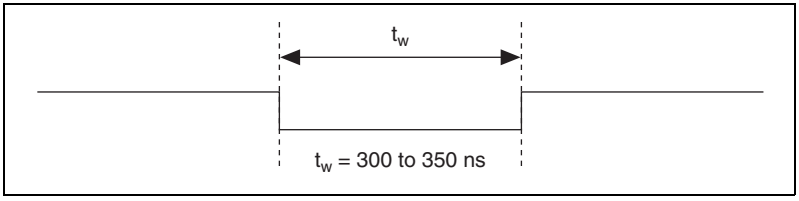


Figure 4-30. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time so that new data can be written to the DAC latches.

The DAQPad-6070E UI counter normally generates UPDATE* unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal buffer counter (BC).

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses UISOURCE as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for UISOURCE in the level-detection mode. Configure the polarity selection for the PFI pin for either active high or active low. Figure 4-31 shows the timing requirements for UISOURCE.

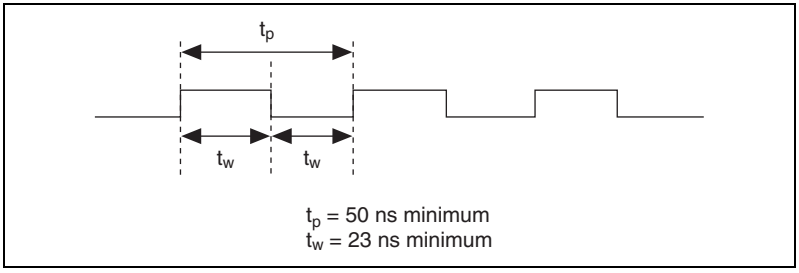


Figure 4-31. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

The 20 MHz or 100 kHz internal timebase generates UISOURCE unless you select an external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, GPCTR0_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI is externally inputting the source clock. This output is set to high-impedance at startup.

Figure 4-32 shows the timing requirements for GPCTR0_SOURCE.

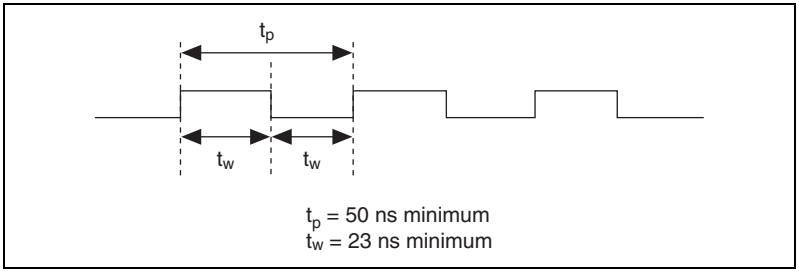


Figure 4-32. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

The 20 MHz or 100 kHz timebase generates GPCTR0_SOURCE unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-33 shows the timing requirements for GPCTR0_GATE.

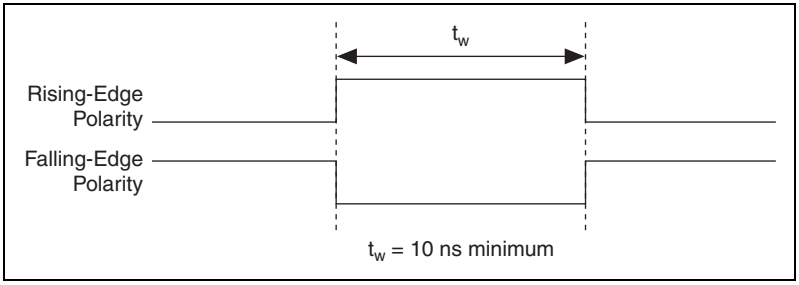


Figure 4-33. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is only available as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup. Figure 4-34 shows the timing of GPCTR0_OUT.

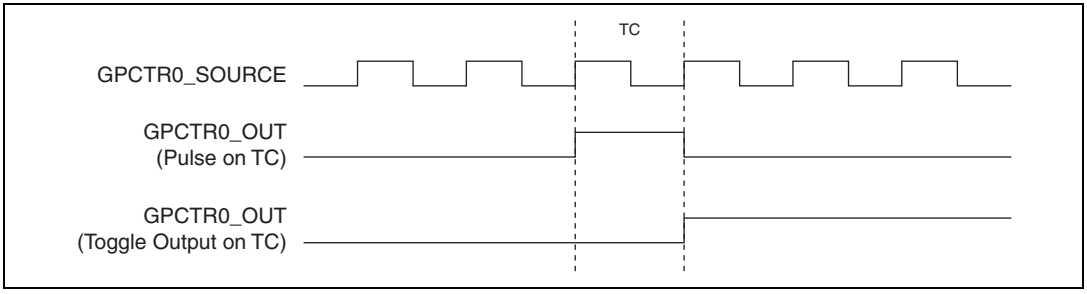


Figure 4-34. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and counts up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if the source clock is externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-35 shows the timing requirements for GPCTR1_SOURCE.

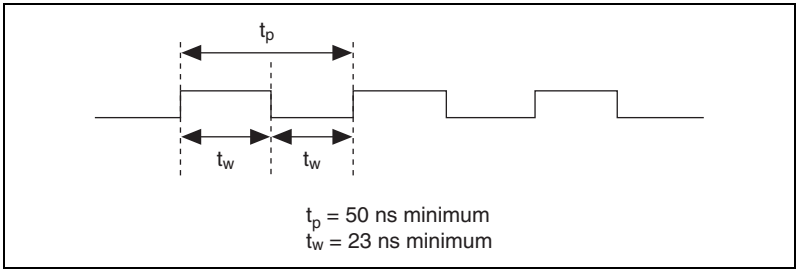


Figure 4-35. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

The 20 MHz or 100 kHz timebase generates the GPCTR1_SOURCE unless you select an external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, GPCTR1_GATE is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR1_GATE monitors the actual gate signal connected to general-purpose counter 1, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-36 shows the timing requirements for GPCTR1_GATE.

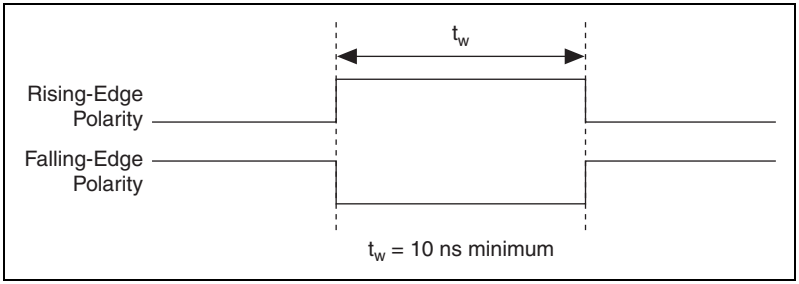


Figure 4-36. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. GPCTR1_OUT monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This signal is set to high-impedance at startup. Figure 4-37 shows the timing requirements for GPCTR1_OUT.

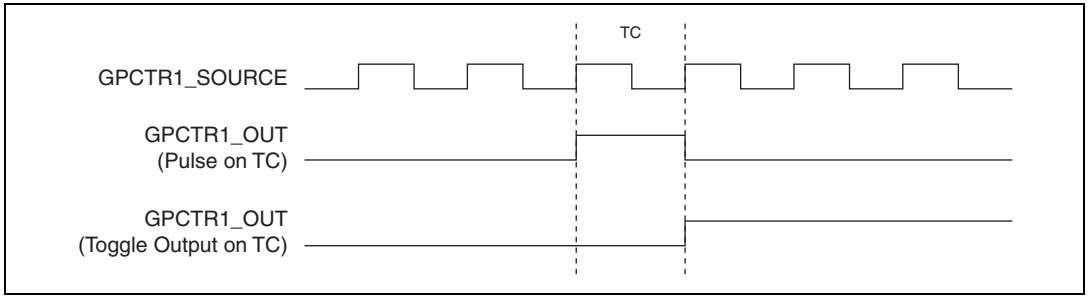


Figure 4-37. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-38 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of the DAQPad-6070E.

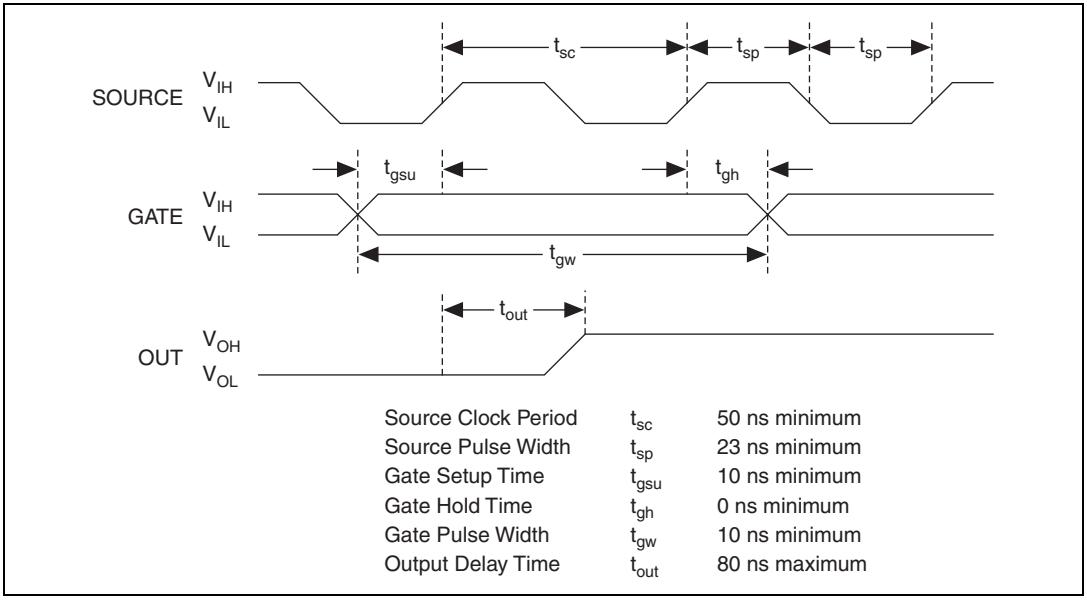


Figure 4-38. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-38 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the DAQPad-6070E. Figure 4-38 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the

gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-38. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied near a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the DAQPad-6070E. Figure 4-38 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The DAQPad-6070E frequency generator outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to high-impedance at startup.

Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the DAQPad-6070E, if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply to AI signal routing to the device and to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use DIFF input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the device. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.

- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a DAQ system is the video monitor. Separate the monitor from the analog signals as far as possible.

The following recommendations apply for all signal connections to your DAQPad-6070E:

- Separate the DAQPad-6070E signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the DAQPad-6070E signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run parallel, or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running the lines through special metal conduits.

For more information, refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals*, available at `ni.com/zone`.

5

Calibration

This chapter discusses the calibration procedures for the DAQPad-6070E. NI-DAQ includes calibration functions for performing all the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the DAQPad-6070E, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for most applications. If you do not calibrate the device, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The DAQPad-6070E is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory-calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

The DAQPad-6070E can measure and correct for almost all of its calibration-related errors without any external signal connections. NI-DAQ provides a self-calibration method. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. The *External Calibration* section addresses this error. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The DAQPad-6070E has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage level is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may want to externally calibrate the device.

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate the device by calling the NI-DAQ calibration function.

To externally calibrate the device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. To calibrate a 12-bit device, the external reference should be at least ±0.015% (±150 ppm) accurate.

For a detailed calibration procedure for the DAQPad-6070E, refer to the *E Series Calibration Procedure* by clicking **Manual Calibration Procedures** at `ni.com/calibration`.

Other Considerations

The CalDACs adjust the gain error of each AO channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the AO gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the AO channel either in software or with external hardware. See Appendix A, *Specifications*, for AO gain error information.

Gain error and offset error are temperature dependent. It can take as long as 30 minutes for the temperature in the device to sufficiently stabilize so the device can be calibrated. Make sure the DAQPad-6070E has been powered on for 30 minutes in a stable temperature environment before calibrating the device. The device should be calibrated at the temperature in which it will operate.

For more information on calibrating the device, refer to `ni.com/calibration`.

A

Specifications

This appendix lists the specifications of the DAQPad-6070E. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential (software-selectable per channel)

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate (single-channel)[1] ..... 1.25 MS/s

Input signal ranges

Channel Gain (Software-Selectable)	Device Range (Software-Selectable)	
	Bipolar	Unipolar
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

[1] Refer to the settling time table in *Dynamic Characteristics* for multichannel rates.

Input coupling.....DC

Max working voltage
(signal and common mode) .....Each input should remain within ±11 V of ground

Overvoltage protection .....±25 V powered on, ±15 V powered off

Inputs protected .....ACH<0..15>, AISENSE

FIFO buffer size.....2,048 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather (single transfer, demand transfer)

Configuration memory size .....512 words

Transfer Characteristics

Relative accuracy.....±0.5 LSB typ dithered, ±1.5 LSB max undithered

DNL .....±0.5 LSB typ, ±1 LSB max

No missing codes.....12 bits, guaranteed

Offset error

Pregain error after calibration.....±12 µV max

Pregain error before calibration.....±2.5 mV max

Postgain error after calibration .....±0.5 mV max

Postgain error before calibration .....±100 mV max

Gain error (relative to calibration reference)

After calibration (gain = 1).....±0.02% of reading max

Before calibration .....±2.5% of reading max

Gain ≠ 1 with gain error
adjusted to 0 at gain = 1.....±0.02% of reading max

Amplifier Characteristics

Input impedance

- Normal powered on ..... 100 GΩ in parallel with 100 pF
- Powered off ..... 820 Ω min
- Overload ..... 820 Ω min

Input bias current ..... ±200 pA

Input offset current ..... ±100 pA

CMRR, all input ranges, DC to 60 Hz

- Gain of 0.5 ..... 95 dB
- Gain of 1 ..... 100 dB
- Gain of ≥2 ..... 106 dB

Dynamic Characteristics

Bandwidth

- Small (–3 dB) ..... 1.6 MHz
- Large (1% THD) ..... 1 MHz

Settling time to full-scale step

Gain	Accuracy*		
	±0.012% (±0.5 LSB)	**±0.024% (±1 LSB)**	**±0.098% (±4 LSB)**
0.5	2 µS typ, 3 µS max	1.5 µS typ, 2 µS max	1.5 µS typ, 2 µS max
1	2 µS typ, 3 µS max	1.5 µS typ, 2 µS max	1.3 µS typ, 1.5 µS max
2 to 50	2 µS typ, 3 µS max	1.5 µS typ, 2 µS max	0.9 µS typ, 1 µS max
100	2 µS typ, 3 µS max	1.5 µS typ, 2 µS max	1 µS typ, 1.5 µS max

* Accuracy values valid for source impedances less than 1 kΩ. Refer to *Multiple Channel Scanning Considerations* for more information.

System noise (LSB_{rms}, not including quantization)

Gain	Dither Off	Dither On
0.5 to 10	0.25	0.5
20	0.4	0.6
50	0.5	0.7
100	0.8	0.9

Crosstalk (DC to 100 kHz)

Adjacent channels.....–75 dB

All other channels.....–90 dB

Stability

Recommended warm-up time.....30 minutes

Offset temperature coefficient

Pregain.....±5 µV/°C

Postgain .....±240 µV/°C

Gain temperature coefficient .....±20 ppm/°C

Onboard calibration reference

Level.....5.000 V (±3.5 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient.....±5 ppm/°C max

Long-term stability .....±15 ppm/$\sqrt{1,000\ h}$

Analog Output

Output Characteristics

Number of channels.....2

Resolution.....12 bits, 1 in 4,096

Max update rate

FIFO Mode		Non-FIFO Mode	
Internally Timed	**Externally Timed**	**1 Channel**	**2 Channels**
1 MS/s	950 kS/s	800 kS/s, system dependent	400 kS/s, system dependent

Type of DAC ..... Double-buffered, multiplying

FIFO buffer size

DAQPad-6070E ..... 2,048 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather (single-transfer, demand transfer)

Transfer Characteristics

Relative accuracy (INL)

After calibration ..... ±0.3 LSB typ, ±0.5 LSB max

Before calibration ..... ±4 LSB max

DNL

After calibration ..... ±0.3 LSB typ, ±1.0 LSB max

Before calibration ..... ±3 LSB max

Monotonicity ..... 12 bits, guaranteed after calibration

Offset error

After calibration ..... ±1.0 mV max

Before calibration ..... ±200 mV max

Gain error (relative to internal reference)

After calibration ..... ±0.01% of output max

Before calibration ..... ±0.5% of output max

Gain error (relative to external reference) .....+0 to +0.5% of output max, not adjustable

Voltage Output

Ranges .....±10 V, 0 to 10 V, ±EXTREF, 0 to EXTREF (software-selectable)

Output coupling .....DC

Output impedance.....0.1 Ω max

Current drive.....±5 mA max

Protection.....Short-circuit to ground

Power-on state .....0 V

External reference input

- Range.....±11 V
- Overvoltage protection .....±25 V powered on, ±15 V powered off
- Input impedance .....10 kΩ
- Bandwidth (–3 dB) .....1 MHz

Dynamic Characteristics

Settling time for full-scale step.....3 µs to ±0.5 LSB accuracy

Slew rate .....20 V/µs

Noise.....200 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

- Magnitude
  - Reglitching disabled.....±20 mV
  - Reglitching enabled.....±4 mV
- Duration.....1.5 µs

Stability

Offset temperature coefficient ..... ±50 µV/°C

Gain temperature coefficient

Internal reference ..... ±25 ppm/°C

External reference ..... ±25 ppm/°C

Onboard calibration reference

Level ..... 5.000 V (±3.5 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient ..... ±5 ppm/°C max

Long-term stability ..... ±15 ppm/$\sqrt{1,000\ \text{h}}$

Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ..... Input (high-impedance)

Data transfers ..... Programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns, edge-detect mode

Min gate pulse duration ..... 10 ns, edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather (single transfer, demand transfer)

Triggers

Analog Trigger

Source ..... ACH<0..15>, external trigger (PFI0/TRIG1)

Level ..... ± full-scale, internal; ±10 V, external

Slope ..... Positive or negative (software-selectable)

Resolution ..... 8 bits, 1 in 256

Hysteresis ..... Programmable

Bandwidth (–3 dB)..... 2 MHz internal, 7 MHz external

External input (PFI0/TRIG1)

Impedance..... 10 kΩ

Coupling..... DC

Protection..... –0.5 to V_{cc} + 0.5 V when configured as a digital signal, ±35 V when configured as an analog trigger signal or disabled, ±35 V powered off

Digital Trigger

Compatibility..... TTL

Response..... Rising or falling edge

Pulse width..... 10 ns min

RTSI

Trigger lines..... 4

Bus Interface

Type..... IEEE 1394, 400 Mbits/s, asynchronous protocol

Power Requirement

Power available at I/O connector..... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions
(not including BNC connector)..... 30.7 by 25.4 by 4.3 cm (12.1 by 10 by 1.7 in.)

I/O connector..... 68-pin male SCSI-II type or 15 BNCs and 30 removable screw terminals

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....±11 V, Installation Category I

Channel-to-channel.....±11 V, Installation Category I

Environmental

Operating temperature .....0 to 55 °C

Storage temperature.....–20 to 70 °C

Relative humidity .....10 to 90%, noncondensing

Maximum altitude.....2000 meters

Pollution degree (indoor use only) 2

Safety

The DAQPad-6070E meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3111-1:1994
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions .....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity .....Evaluated to EN 61326:1997/
A1:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click Declaration of Conformity at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate

product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

Optional Cable Connector Descriptions

This appendix describes the connectors on the optional cables for the DAQPad-6070E with mass termination.

Figure B-1 shows the pin assignments for the 68-pin E Series connector. This connector is available when you use the SH6868 or R6868 cable assemblies with the DAQPad-6070E.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure B-1. 68-Pin E Series Connector Pin Assignments

Figure B-2 shows the pin assignments for the 50-pin E Series connector. This connector is available when you use the SH6850 or R6850 cable assemblies with the DAQPad-6070E.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5 V
+5 V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PRI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-2. 50-Pin E Series Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers, relating to usage and special features of the DAQPad-6070E.

General Information

What is the DAQPad-6070E?

The DAQPad-6070E is a switchless, jumperless enhanced MIO device for IEEE 1394 that uses the DAQ-STC for timing.

What is the DAQ-STC?

The DAQ-STC is the system-timing control application-specific integrated circuit (ASIC) designed by NI, and it is the backbone of the DAQPad-6070E. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- AI—two 24-bit, two 16-bit counters
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. Capabilities such as buffered pulse generation, equivalent time sampling, and seamless sampling rate change are possible.

What does sampling rate mean to me?

The sampling rate is the fastest you can acquire data on your device and still achieve accurate results. For example, the DAQPad-6070E has a sampling rate of 20 kS/s. This sampling rate is aggregate: one channel at 20 kS/s or two channels at 10 kS/s per channel illustrates the relationship. Notice, however, that the DAQPad-6070E has settling times that vary with gain and accuracy. See Appendix A, *Specifications*, for exact specifications.

What type of 5 V protection does the DAQPad-6070E have?

The DAQPad-6070E has 5 V lines equipped with a self-resetting 1 A fuse.

How do I use the DAQPad-6070E with the NI-DAQ C API?

The *NI-DAQ User Manual* describes the general programming flow and provides example code for using the NI-DAQ API. For a list of functions that support the NI PCI-6110/6111, you can refer to the *NI-DAQ Function Reference Help* (for NI-DAQ version 6.7 or later) or the *NI-DAQ Function Reference Manual* (for NI-DAQ version 6.6 or earlier).

The DAQPad-6070E is periodically cycling the power. What does this mean?

If the DAQPad is periodically cycling the power, this means that the DAQPad is powered on, but it does not detect a link between the computer and the DAQPad.

Installing and Configuring

What jumpers should I be aware of when configuring the DAQPad-6070E?

The DAQPad-6070E is jumperless and switchless.

Which NI document should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* and the NI-DAQ or application software release notes documentation are good places to start.

What is FireWire?

FireWire and IEEE 1394 are the same thing. FireWire was the original name when the technology was developed by Apple Computer. Later, Apple turned over the specification to the IEEE for standardization.

Can I use a 400 Mbits/s 1394 device with a 100 Mbits/s device?

Yes. However, the bus slows to the slowest speed. So, the 400 Mbits/s 1394 device will operate faster if the 100 Mbits/s device is removed from the bus.

How many devices can I hook up to a 1394 bus?

Up to 64 different devices, including the PC, may be attached to a single bus.

Can I connect the 1394 bus any way I want?

No. You cannot have cycles in the bus cabling, and you must have fewer than 16 hops between devices.

Do I need any external hardware to connect (daisy-chain) multiple DAQPad-6070Es?

No, all you need is the computer, the DAQPads, and one 1394 cable for each DAQPad. 1394 allows you to daisy-chain devices without any additional hardware.

My computer has a FireWire port that uses a 4-pin connection, and the 1394 uses a 6-pin connection. How can I connect my computer to the DAQPad-6070E?

If you are using a computer that has a 4-pin FireWire port, you must purchase a 6- to 4-pin adapter to install the DAQPad-6070E. The difference between the 4- and 6-pin ports is that 4-pin ports do not have power supplied to them through the port. Since the DAQPad-6070E does not use power through the firewire port, using a 6- to 4-pin converter does not have an impact on the performance or functionality of the DAQPad.

What can I do to optimize the performance of the 1394 device?

You can do several things to optimize the performance of the 1394 device. First, try to keep your bus running at the fastest speed possible by attaching only devices that are at least as fast as the 1394 device. If a 200 M/s device is added to the bus with the 400 M/s DAQ device, you slow the entire bus to 200 M/s. Second, minimize the maximum number of hops between the devices on the bus. The more hops you have, the slower the bus runs. Finally, remember there is only a limited amount of bandwidth available on the bus. If you stream DV at 20 M/s, you can hurt DAQ performance.

What is the best way to test the DAQPad-6070E without programming the device?

If you are using Windows, Measurement & Automation Explorer (MAX) has a Test Panel option that is available by selecting **Devices and Interfaces** in the left-hand panel and then selecting the device. The Test Panels are excellent tools for performing simple functional tests of the

device, such as AI, DIO, and counter/timer tests. If you are using Mac OS, the NI-DAQ Configuration Utility provides the same functionality.

Analog Input and Output

I'm using the device in DIFF input mode, and I connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check the ground reference connections. The signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

I am seeing crosstalk or ghost voltages when sampling multiple channels. What does this mean?

You may be experiencing a phenomenon called charge injection. Charge injection occurs when you sample a series of high-output impedance sources with a multiplexer. Multiplexers contain switches, usually made of switched capacitors. When one channel is selected in a multiplexer, those capacitors accumulate charge. When the next channel is selected, the accumulated charge leaks backward through that channel. If the output impedance of the source connected to the second channel is high enough, the resulting reading can somewhat reflect the voltage trends in the first channel.

To solve this problem, you must either use a voltage follower (op-amp with unity gain) for each high-impedance source before connecting to the DAQ device or decrease the sample rate.

Another common cause of channel crosstalk is caused by sampling multiple channels at various gains. In this situation, the settling times may increase. For more information on charge injection and sampling channels at different gains, refer to the *Multiple Channel Scanning Considerations* section in Chapter 3, *Hardware Overview*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when switching the most significant bit (MSB) of the D/A code. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of your output signal. The DAQPad-6070E has built-in reglitchers, which can be software-enabled, on its AO channels. Refer to the *Analog Output Reglitch Selection* section in Chapter 3, *Hardware Overview*, for more information about reglitching.

Can I synchronize a one-channel AI data acquisition with a one-channel AO waveform generation on the DAQPad-6070E?

Yes. One way to synchronize is to use the waveform generation timing pulses to control the AI data acquisition. To do this, follow steps 1 through 4, in addition to the usual steps for data acquisition and waveform generation configuration:

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal (deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal (deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate AI data acquisition, which starts only when the AO waveform generation starts.
4. Initiate AO waveform generation.

Can I programmatically enable different channels on an E Series device to acquire in different modes? For example, can channel 0 be in DIFF mode and channel 1 be in RSE mode?

Different channels on E Series devices can be enabled to acquire in different modes. However, different pairs of channels are used in different modes. In the configuration mentioned in the question above, ACH0 and ACH8 would be configured in DIFF mode, and ACH1 and AIGND would be configured in RSE mode. In this configuration, ACH8 could not be used in a single-ended configuration.

To enable multi-mode scanning in LabVIEW, you would use the coupling & input config cluster input of the AI Config VI. This input has a one-to-one correspondence with the channels array input of the AI Config VI. Therefore, you must list all channels either individually or in groups of channels with the same input configuration. For example, if you want channel 0 to be DIFF and channels 1 and 2 to be RSE, Figure C-1 demonstrates how to program this configuration in LabVIEW.

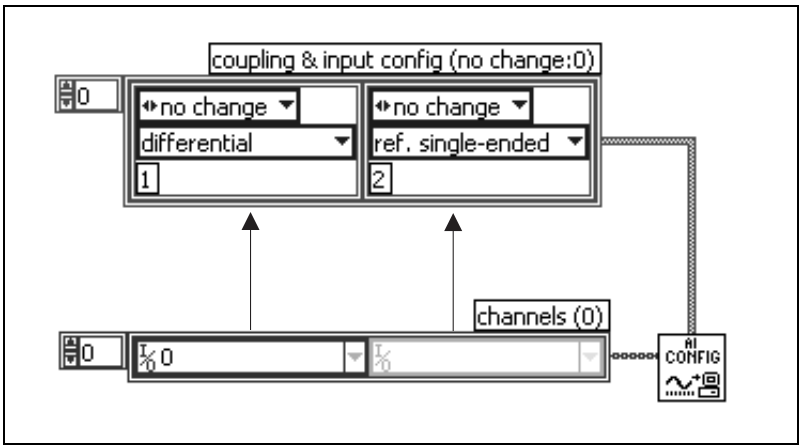


Figure C-1. Configuring Channels for Different Acquisition Modes in LabVIEW

To enable multi-mode scanning when using NI-DAQ function calls, call the `AI_Configure` function for each channel.

How can I use the STARTSCAN and CONVERT* signals on the DAQPad-6070E to sample AI channels?

E Series devices use both the STARTSCAN and CONVERT* signals to perform interval sampling. STARTSCAN, output by the DAQ-STC, controls the *scan interval* (1/scan interval = scan rate), and CONVERT* controls the *interchannel delay* (1/interchannel delay = sampling rate).

This relationship is shown in Figure C-2. This method allows multiple channels to be sampled relatively quickly in relationship to the overall scan rate. The effect of this method is a pseudo-simultaneous effect with a fixed delay between channels.

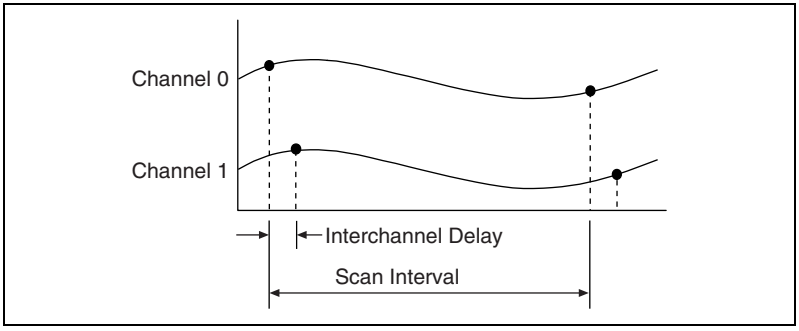


Figure C-2. Interchannel Delay and Scan Interval

Timing and Digital I/O

What types of triggering can be hardware-implemented on the DAQPad-6070E?

Digital triggering is hardware-supported on every DAQPad-6070E. In addition, the DAQPad-6070E supports hardware analog triggering.

What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO devices have a 20 MHz timebase. The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

Will the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs do still run. However, there are many differences in the counters between the DAQPad-6070E and other devices; the counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using NI-DAQ or LabWindows/CVI, the counter/timer applications that you wrote previously do not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions do not work with the DAQ-STC. The GPCTR functions add functionality to the ICTR and CTR functions, but you must rewrite the application with the GPCTR function calls.

I am using one of the general-purpose counter/timers on the DAQPad-6070E, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using NI-DAQ or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are high-impedance.

What are the PFIs, and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode

Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Table C-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
TRIG1	AI Start Trigger	ND_IN_START_TRIGGER
TRIG2	AI Stop Trigger	ND_IN_STOP_TRIGGER
STARTSCAN	AI Scan Start	ND_IN_SCAN_START
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
CONVERT*	AI Convert	ND_IN_CONVERT
AIGATE	—	ND_IN_EXTERNAL_GATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER
UPDATE*	AO Update	ND_OUT_UPDATE
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
AOGATE	—	ND_OUT_EXTERNAL_GATE

Caution If you enable a PFI line for output, do *not* connect any external signal sources to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high-impedance by the hardware. This setting means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-2, *I/O Signal Summary for the DAQPad-6070E*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) is in the high-impedance state after power on, and Table 4-2 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the DIO(0) pin to a logic high when the output is in a high-impedance state.

D

Technical Support and Professional Services

Visit the following sections of the NI Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meaning	Value
p-	pico	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

°	degrees
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
–	negative of, or minus
Ω	ohms
/	per
%	percent
±	plus or minus
+	positive of, or plus
$\sqrt{\ }$	square root of
+5 V	+5 VDC source signal

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH	analog input channel signal
ACH0GND	analog input channel ground signal
ActiveX controls	a special form of Automation Object. ActiveX Controls are similar to Visual Basic custom controls (VBXs), but their architecture is based on OLE; ActiveX Controls can be freely plugged into any OLE-enabled development tool, application, or Web browser.
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADE	application development environment
AI	analog input
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions

B

BC	buffer counter
bipolar	a signal range that includes both positive and negative values (for example, –5 to +5 V)
BNC	refers to a coaxial connector

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels
channel rate	reciprocal of the interchannel delay
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
common-mode noise	unwanted signals that appear in equal phase and amplitude on both teh inverting and noninverting input in a differential measurement system. Ideally, but not completely in practice, the measurement device ignores this noise, because the measurement device is designed to respond to the difference between the inverting and noninverting inputs.
common-mode range	input range over which a circuit can handle a common-mode signal without overload or errors
common-mode signal	a signal, relative to the instrument chassis or computer's ground, of the signals from a differential input. This is often a noise signal, such as 50 or 60 Hz hum.

common-mode voltage	any voltage present at both instrumentation amplifier inputs with respect to amplifier ground
CONVERT*	convert signal
counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
DAQ-STC	data acquisition system timing controller chip
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential input mode
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.

DNL	differential nonlinearity—a measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output
DOC	the Canadian Department of Communications
DoC	Declaration of Conformity

E

edge detection	a technique that locates an edge of an analog signal, such as the edge of the square wave
EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EMC	electromechanical compliance
ENOB	effective number of bits—a measure of the actual performance of an ADC after its various noise sources and nonlinearities are included. The ENOB is computed as the signal-to-noise ratio of the ADC (in dB) minus 1.76, divided by 6.02. Also called effective bits.
ESD	electrostatic discharge—a high-voltage, low-current discharge of static electricity that can damage sensitive electronic components. Electrostatic discharge voltage can easily range from 1,000 to 10,000 V.
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

F	farads
FCC	Federal Communications Commission

FIFO	first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
floating signal source	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
FREQ_OUT	frequency output signal
FS	floating source
ft	feet

G

gain	factor by which a signal is amplified, often expressed in dB
GATE	gate signal
glitch	an unwanted momentary deviation from a desired signal
GPCTR	general-purpose counter
GPCTR0_GATE	general-purpose counter 0 gate signal
GPCTR0_OUT	general-purpose counter 0 output signal
GPCTR0_SOURCE	general-purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general-purpose counter 0 up down
GPCTR1_GATE	general-purpose counter 1 gate signal
GPCTR1_OUT	general-purpose counter 1 output signal

GPCTR1_SOURCE	general-purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general-purpose counter 1 up down
grounded signal source	a source that is connected to the building system ground. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.
GS	grounded source

H

h	hour
hex	hexadecimal
hysteresis	lag between making a change and the effect of the change
Hz	hertz

I

IEEE	Institute of Electrical and Electronic Engineers
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low
impedance	electrical characteristic of a circuit, expressed in ohms and/or capacitance/inductance
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry

interchannel delay	amount of time that passes between sampling consecutive channels. The interchannel delay must be short enough to allow sampling of all the channels in the channel list, within the scan interval. The greater the interchannel delay, the more time the PGIA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by CONVERT*.
IRQ	interrupt request

K

k	kilo
kS/s	1,000 samples per second

L

LabVIEW	a graphical programming language
LED	light-emitting diode—used to show device status
library	a file containing compiled object modules, each comprised of one or more functions that can be linked to other object modules that make use of these functions. NIDAQ32.LIB is a library that contains NI-DAQ functions. The NI-DAQ function set is broken down into object modules so that only the object modules that are relevant to your application are linked in, while those object modules that are not relevant are not linked.
linearity	the adherence of device response to the equation R = KS, where R = response, S = stimulus, and K = a constant
LSB	least significant bit

M

m	meter
M	the standard metric prefix for 1 million or 10^6, when used with units of measure, such as volts and hertz
mass termination	signal connection via a large pin count connector as opposed to connection via many small connectors or screw terminals

MB	megabytes
Mbytes/s	megabytes per second
Measurement & Automation Explorer (MAX)	a controlled centralized configuration environment that allows you to configure all your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices
MIO	multifunction I/O
MITE	MXI Interfaces to Everything
MS	million samples
MS/s	1,000,000 samples per second
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel
mV	millivolts

N

NC	not connected
NI	National Instruments
NI-DAQ	NI driver software for DAQ hardware
noise	an undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
nonreferenced signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common example of nonreferenced signal sources are batteries, transformers, or thermocouples.

NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
pd	pull-down
PFI	Programmable Function Input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general-purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general-purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_SOURCE	PFI8/general-purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general-purpose counter 0 gate
PGIA	Programmable Gain Instrumentation Amplifier

Plug and Play devices	devices that do not require DIP switches or jumpers to configure resources on the devices—also called switchless devices
posttriggering	the technique used on a DAQ device to acquire a programmed number of samples after trigger conditions are met
potentiometer	an electrical device the resistance of which can be manually adjusted; used for manual adjustment of electrical circuits and as a transducer for linear or rotary position
port	a digital port, consisting of four or eight lines of digital input and/or output
ppm	parts per million
precision	the measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
pretriggering	the technique used on a DAQ device to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition
pseudodifferential input	pseudodifferential input channels are all referred to a common ground, but this ground is not directly connected to the computer ground
pu	pull up

R

RAM	random access memory
range	the maxiumum and minimum parameters between which a sensor, instrument, or device operates with a specified set of characteristics
referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground. Also called grounded signal sources.
reglitch	(1) to modify the glitches in a signal in order to make them less disruptive; (2) circuitry used on analog outputs to generate uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum.

resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
RH	relative humidity
rms	root mean square
RSE	referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions
RTSI_OSC	RTSI Oscillator—RTSI bus master clock

S

s	seconds
S	samples
S/s	samples per second—used to express the rate at which a DAQ board samples an analog signal
SC	scan counter
scan interval	controls how often a scan is initialized. The scan interval is regulated by STARTSCAN.
scan rate	reciprocal of the scan interval
SCANCLK	scan clock signal
SCSI	Small Computer System Interface—a high-speed, peripheral-connect interface primarily used for hard disks, CD-ROM drives, tape drives, and other mass-storage devices to PCs

SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy computer environment
settling time	the amount of time required for a voltage to reach its final value within specified limits
signal conditioning	the manipulation of signals to prepare them for digitizing
SI2	sample interval counter
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
SOURCE	source signal
source impedance	a parameter of signal sources that reflects current-driving ability of voltage sources (lower is better) and the voltage-driving ability of current sources (higher is better)
STARTSCAN	start scan signal
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count—the ending value of a counter
t_d	delay time
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibels (dB) or percent
thermocouple	a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.

TIO	timing I/O
t_{off}	an offset (delayed) pulse; the offset is t nanoseconds from the falling edge of the CONVERT* signal
t_{out}	output delay time
t_p	pulse period
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-to-transistor logic
t_w	pulse width

U

UI	update interval counter
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
UPDATE	update signal

V

V	volts
V_{cc}	positive voltage supply
V_{cm}	common-mode noise
VDC	volts direct current

VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
Vrms	volts, root mean square
V_s	signal source

W

waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal

Index

Symbols

Numerics

A

B

C

D

E

F

G

H

I

K

L

M

N

O

P

Q

R

S

T

U

V

W